1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J95 MLB SKL

LAST_MODIFICATION=Thu Feb 26 18:38:23 2015

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
4	0003859507	ENGINEERING RELEASED	2015-02-26

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90	105	GRAPHICS: GPU VDDCI VR	hcheng_j95	02/10/2015
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DRAWING

TITLE=J95_skl_am
ABBREV=DRAWING
LAST_MODIFIED=Thu Feb 26 18:38:23 2015

J95,SCHEM,MLB_SKL_AM

DRAWING TITLE: SCHEM,MLB SKL,J95

Apple Inc.

DRAWING NUMBER: 051-00321 | SIZE: D
REVISION: 4.0.0
BRANCH: proto1b
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DRAWING

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
985-00041	PCBA,DEV,MLB_SKL,J95	DEVELOPMENT,J95_DEVEL
685-00059	PCBA,MLB_SKL,COMMON PARTS,J95	J95_COMMON
639-00847	PCBA,MLB SKL,AMETHYST PROA,VRAM_HYNIX,2GB,J95	J95,MLB_CMNPTS,CPU:ULT,SSD:Y,GPU:AM_PROA,FB:2G_HYNIX,EEEE:G99J
639-00846	PCBA,MLB SKL,AMETHYST PROA,VRAM_ELPIDA,2GB,J95	J95,MLB_CMNPTS,CPU:ULT,SSD:Y,GPU:AM_PROA,FB:2G_ELPIDA,EEEE:GCP9
639-00849	PCBA,MLB SKL,AMETHYST XTA,VRAM_HYNIX,4GB,J95	J95,MLB_CMNPTS,CPU:ULT,SSD:Y,GPU:AM_XTA,FB:4G_HYNIX,EEEE:GCR6
639-00848	PCBA,MLB SKL,AMETHYST XTA,VRAM_ELPIDA,4GB,J95	J95,MLB_CMNPTS,CPU:ULT,SSD:Y,GPU:AM_XTA,FB:4G_ELPIDA,EEEE:GCR7
639-01033	PCBA,MLB SKL,CTO,AMETHYST PROA,VRAM_HYNIX,2GB,J95	J95,MLB_CMNPTS,CPU:CTO,SSD:Y,GPU:AM_PROA,FB:2G_HYNIX,EEEE:G99J
639-01032	PCBA,MLB SKL,CTO,AMETHYST PROA,VRAM_ELPIDA,2GB,J95	J95,MLB_CMNPTS,CPU:CTO,SSD:Y,GPU:AM_PROA,FB:2G_ELPIDA,EEEE:GCP9
639-01035	PCBA,MLB SKL,CTO,AMETHYST XTA,VRAM_HYNIX,4GB,J95	J95,MLB_CMNPTS,CPU:CTO,SSD:Y,GPU:AM_XTA,FB:4G_HYNIX,EEEE:GCR6
639-01034	PCBA,MLB SKL,CTO,AMETHYST XTA,VRAM_ELPIDA,4GB,J95	J95,MLB_CMNPTS,CPU:CTO,SSD:Y,GPU:AM_XTA,FB:4G_ELPIDA,EEEE:GCR7

BOM Groups

BOM GROUP	BOM OPTIONS
J95_COMMON	COMMON,ALTERNATE,J95_PROGPARTS,GPU_AM_EM,XDP,SPEAKERID,FBVDDQ_DFLT:1V5,SMCREG:SUP,VR_BULKCAP:CURRENT,GPU:AME_NEP
J95_PROGPARTS	SMC:PROG,BOOTROM:PROG,TBTROM:PROG,CIVROM:PROG,CAMROM:PROG
J95_DEVEL	XDP_CONN,T112,DEVEL_AUDIO

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00122	1	CPU,SKL,QWQF,ES2,Q0,2.6,95W,LGA1151	CPU	CRITICAL	CPU:CTO
337S00114	1	CPU,SKL,QWBE,ES,P0,4/2,2.2,95W,LGA1151	CPU	CRITICAL	CPU:ULT
337S00121	1	CPU,SKL,QWQG,ES2,Q0,2.2,65W,LGA1151	CPU	CRITICAL	CPU:BEST

CPU SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S00002	1	SOCKET.MOLEX,LGA1151,H4	U0500	CRITICAL	

ASICs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00124	1	IC,PCH-H,SKL,SUPRSKU,C0,QHPT,ES2,BGA1151	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
343S0616	1	IC,BCM57766A1,ENET&SD,8X8	U3900	CRITICAL	

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S00058	1	IC,EFI,V0174,J78	U5210	CRITICAL	BOOTROM:PROG
335S00006	1	IC,64 MBIT SPI SERIAL FLASH	U5210	CRITICAL	BOOTROM:BLANK
341S00236	1	IC,SMC-B1,EXTERNAL,VXXXX,POC-S,J78AM	U5000	CRITICAL	SMC:PROG
338S1214	1	IC,SMC12-B1,40MHZ/500MIPS,MCU,1578GA	U5000	CRITICAL	SMC:BLANK
341S00152	1	IC,T29,EPROM,FR,VTBD,POC,J95	U2890	CRITICAL	TBTROM:PROG
335S0915	1	IC,SRL SPI FLASH ROM,4MBIT,50MHZ,USON8	U2890	CRITICAL	TBTROM:BLANK
341S3912	1	IC,ENET ROM,NUMONYX,V1.15,J16/J16G/J17	U3990	CRITICAL	CIVROM:PROG
335S0854	1	1-MBIT,SPI FLASH ROM SOIC, HF	U3990	CRITICAL	CIVROM:BLANK
341S3778	1	IC,CAMERA FLASH,V7230,J16/J17	U4202	CRITICAL	CAMROM:PROG
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7896	1	LABEL,MLB,2D	EEEE_G99J	CRITICAL	EEEE:G99J
825-7896	1	LABEL,MLB,2D	EEEE_GCP9	CRITICAL	EEEE:GCP9
825-7896	1	LABEL,MLB,2D	EEEE_GCR6	CRITICAL	EEEE:GCR6
825-7896	1	LABEL,MLB,2D	EEEE_GCR7	CRITICAL	EEEE:GCR7

J95 SCHEMATIC / PCB #'S

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-00321	1	SCH,MLB SKL,J95	SCH1	CRITICAL	J95
820-00134	1	PCBF,MLB SKL,J95	PCB1	CRITICAL	J95
685-00059	1	PCBA,MLB SKL COMMON PARTS,J95	CMNPTS	CRITICAL	MLB_CMNPTS

J95 ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0147	377S0126		ALL	USB Diode Array
197S0481	197S0480		ALL	25MHX PCH XTAL
197S0479	197S0478		ALL	12MHZ CAM/NXP XTAL
372S0186	372S0185		ALL	Alternate Temp Diode
107S00030	107S00029		ALL	Alt 5mOhm sense
107S0255	107S0240		ALL	Alt 1mOhm sense
341S00016	341S3912		U3990	IC,ENETROM,ADESTO,V1,15,J78
138S0681	138S0638		ALL	10uF Caps
138S0860	138S0775		ALL	Single-source 1uF 402
128S0398	128S0220		ALL	3.3V INPUT CAP
378S0391	378S0390		ALL	DEGUG LEDS
311S00008	311S0271		ALL	AND GATE
155S0830	155S0316		ALL	FERR BD,600 OHM,25,0.5A
376S00016	376S0644		ALL	MOSFET,P-CH,20V,1A
376S00001	376S0659		ALL	MOSFET,P-CH,20V
376S00015	376S0610		ALL	XSTR,FET,DL NCH,60V
138S1103	138S0719		ALL	4.7uF 0402
311S00004	311S0370		ALL	Config. Logic Gate
311S00075	311S0377		ALL	AND GATE
132S0447	132S0448		ALL	0.1uF 0201
138S0855	138S0750		ALL	4.7uF 0402
353S00095	353S3328		ALL	2:4 Diff MUX
311S00072	311S0657		ALL	Dual 2 INP AND GATE

GPU and VRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00081	1	IC,GPU,AMD,P5,AMST,XTA,ES,256B,BGA1737	U8700	CRITICAL	GPU:AM_XTA
337S00082	1	IC,GPU,AMD,P5,AMST,PROA,ES,256B,BGA1737	U8700	CRITICAL	GPU:AM_PROA
333S00027	4	IC,GDDR5,4GBIT,128MX32,5GBPS,GEMMA	U9200,U9250,U9300,U9350	CRITICAL	FB:4G_HYNIX
333S00027	4	IC,GDDR5,4GBIT,128MX32,5GBPS,GEMMA	U9400,U9450,U9500,U9550	CRITICAL	FB:4G_HYNIX
333S0766	4	IC,GDDR5,4GBIT,128MX32,5GBPS,GEMMA	U9200,U9250,U9300,U9350	CRITICAL	FB:4G_ELPIDA
333S0766	4	IC,GDDR5,4GBIT,128MX32,5GBPS,GEMMA	U9400,U9450,U9500,U9550	CRITICAL	FB:4G_ELPIDA
333S0734	4	IC,GDDR5,2GBIT,64MX32,6GBPS,29NM	U9200,U9250,U9300,U9350	CRITICAL	FB:2G_HYNIX
333S0734	4	IC,GDDR5,2GBIT,64MX32,6GBPS,29NM	U9400,U9450,U9500,U9550	CRITICAL	FB:2G_HYNIX
333S0701	4	IC,GDDR5,2GBIT,64MX32,6GBPS,38NM	U9200,U9250,U9300,U9350	CRITICAL	FB:2G_ELPIDA
333S0701	4	IC,GDDR5,2GBIT,64MX32,6GBPS,38NM	U9400,U9450,U9500,U9550	CRITICAL	FB:2G_ELPIDA

SYNC_MASTER=J17_DINI SYNC_DATE=03/15/2013

PAGE TITLE
BOM Configuration

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DRAWING NUMBER 051-00321 SIZE D
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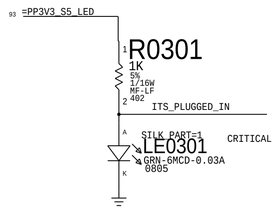
S5 Led



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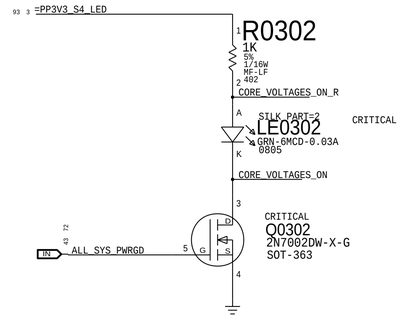

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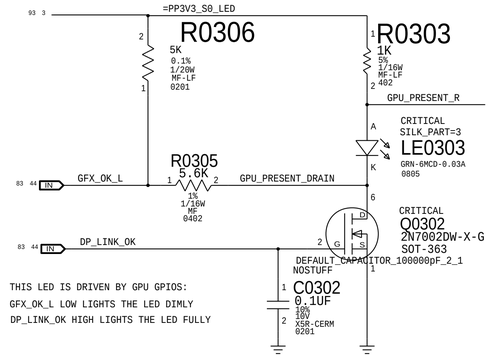

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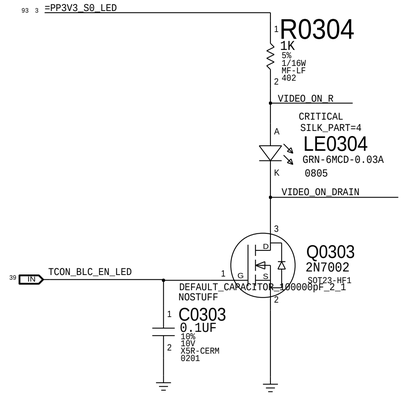

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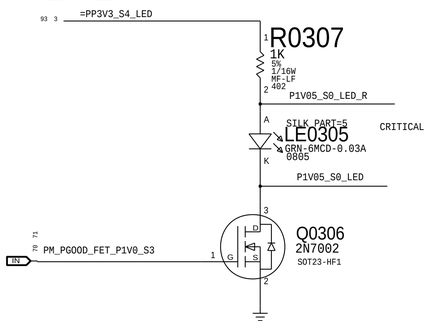

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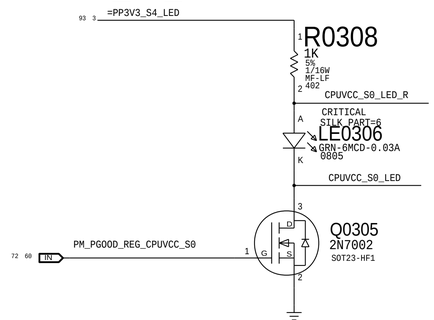

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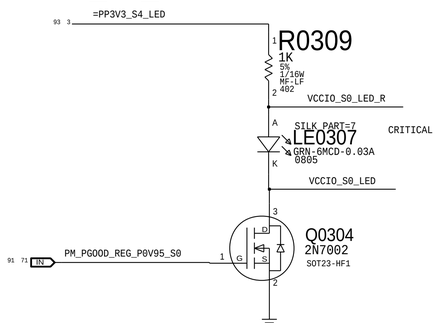

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PAGE TITLE

DEBUG: LEDs

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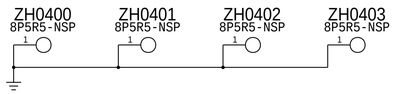
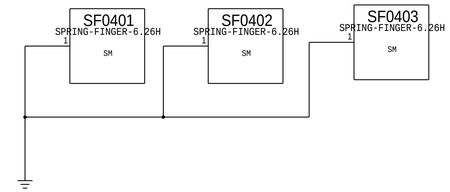
CPU Heatsink

4MM PLATED HOLES (998-4158)



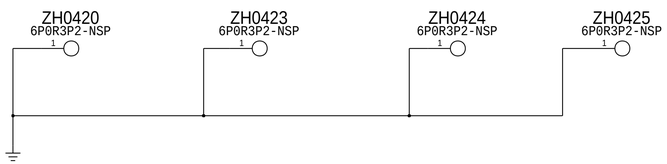
Display EMI Springs

APN: 870-00886



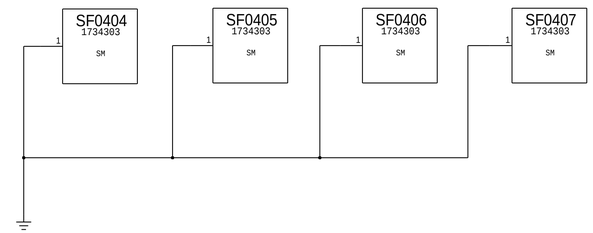
GPU HEATSINK MOUNTING FEATURES

(998-5013. PLATED HOLE, 3.2MM DIA, 6MM PAD TOP/BOT)



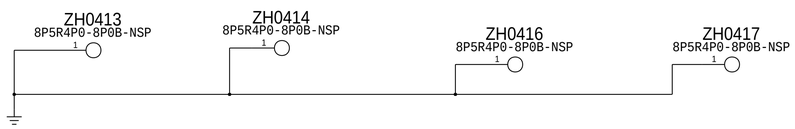
VRAM EMI Springs

APN: 870-00907



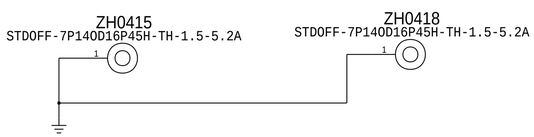
Rear Cover

998-5014 (PLATED HOLES, 4MM DRILL, 8.5MM TOP, 8MM BOT)



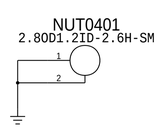
Rear Cover

860-5674 (PCB STANDOFF)



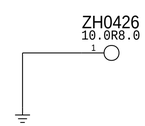
T29 BUMPER

APN: 860-00201



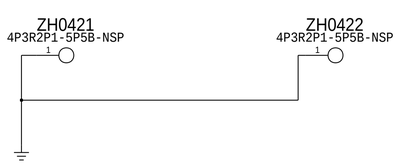
HEATPIPE MTG HOLES

998-5527 (PLATED HOLES, 8MM DIA, 10MM PAD)



X238D WIRELESS CARD MTG HOLES

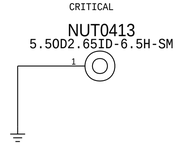
998-01489 (PLATED HOLES, 2.1MM INNER DIAMETER, 5.5MM PAD)



SSD STANDOFF

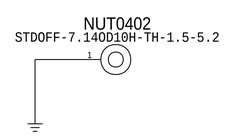
APN: 860-00198

CRITICAL



LOL Boss

860-5675 (PLATED HOLE, 8.41mm pad Top, 8mm pad Bot)



SYNC_MASTER=J17_MAX SYNC_DATE=02/11/2013

PAGE TITLE
MECHANICAL: Holes/PD parts

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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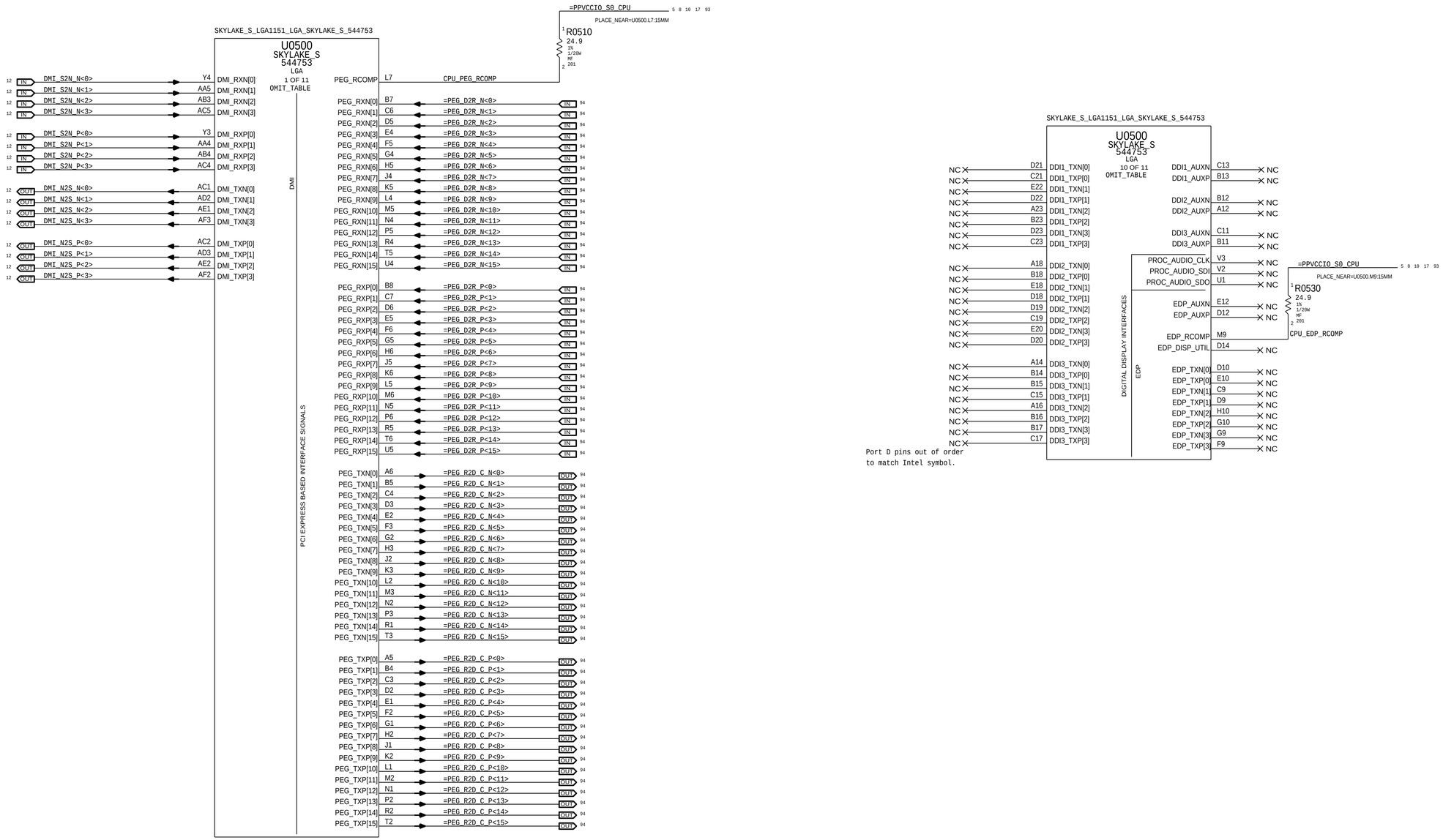

SYNC_MASTER=J78_MLB SYNC_DATE=06/30/2014

PAGE TITLE

CPU & CHIPSET: CPU DMI/PEG/FDI/RSVD

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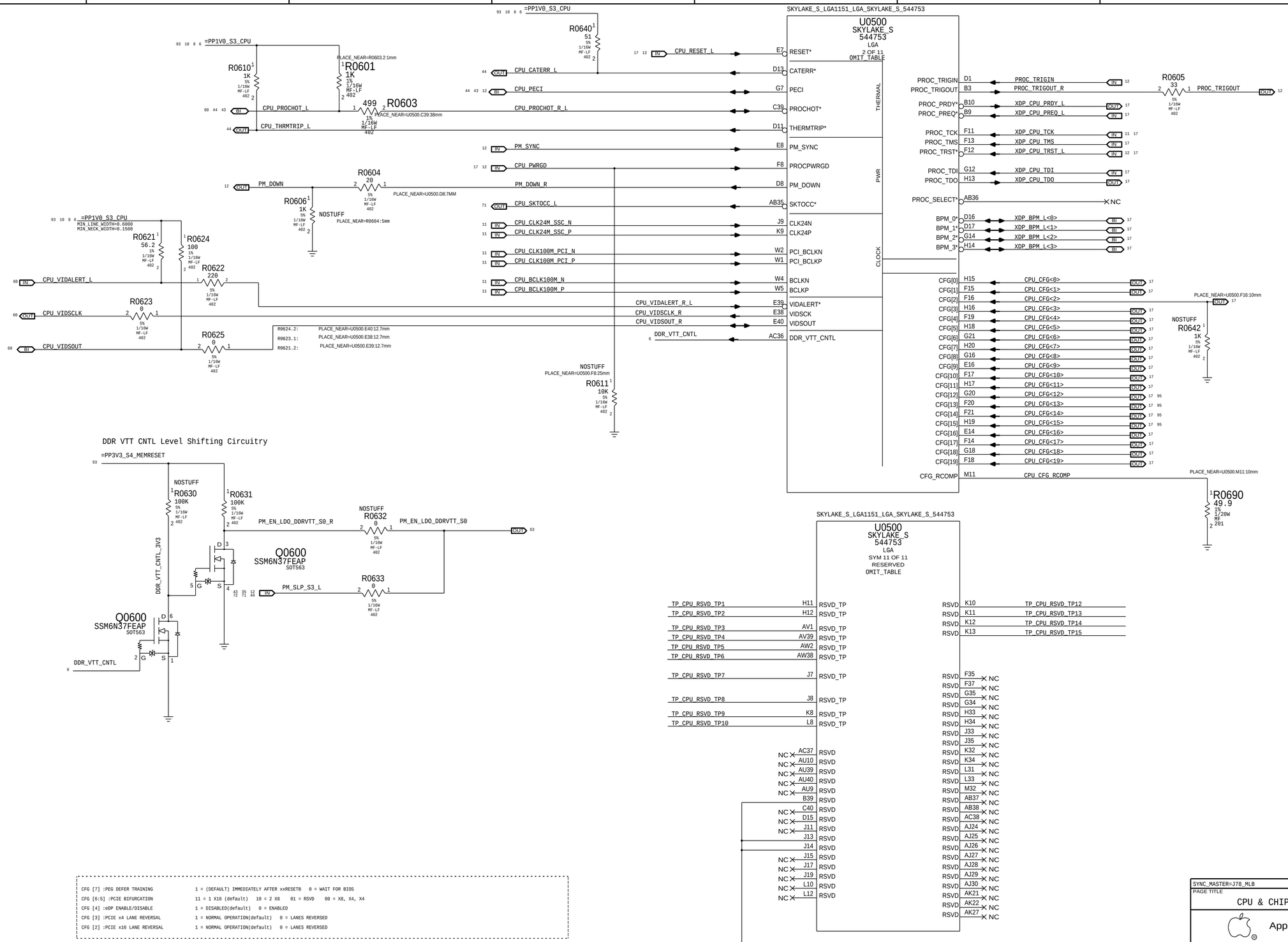

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (default) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED(default) 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION(default) 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION(default) 0 = LANES REVERSED

SYNC_MASTER=J78_MLB SYNC_DATE=06/30/2014

PAGE TITLE

CPU & CHIPSET: CPU Clock/Misc/JTAG/CFG

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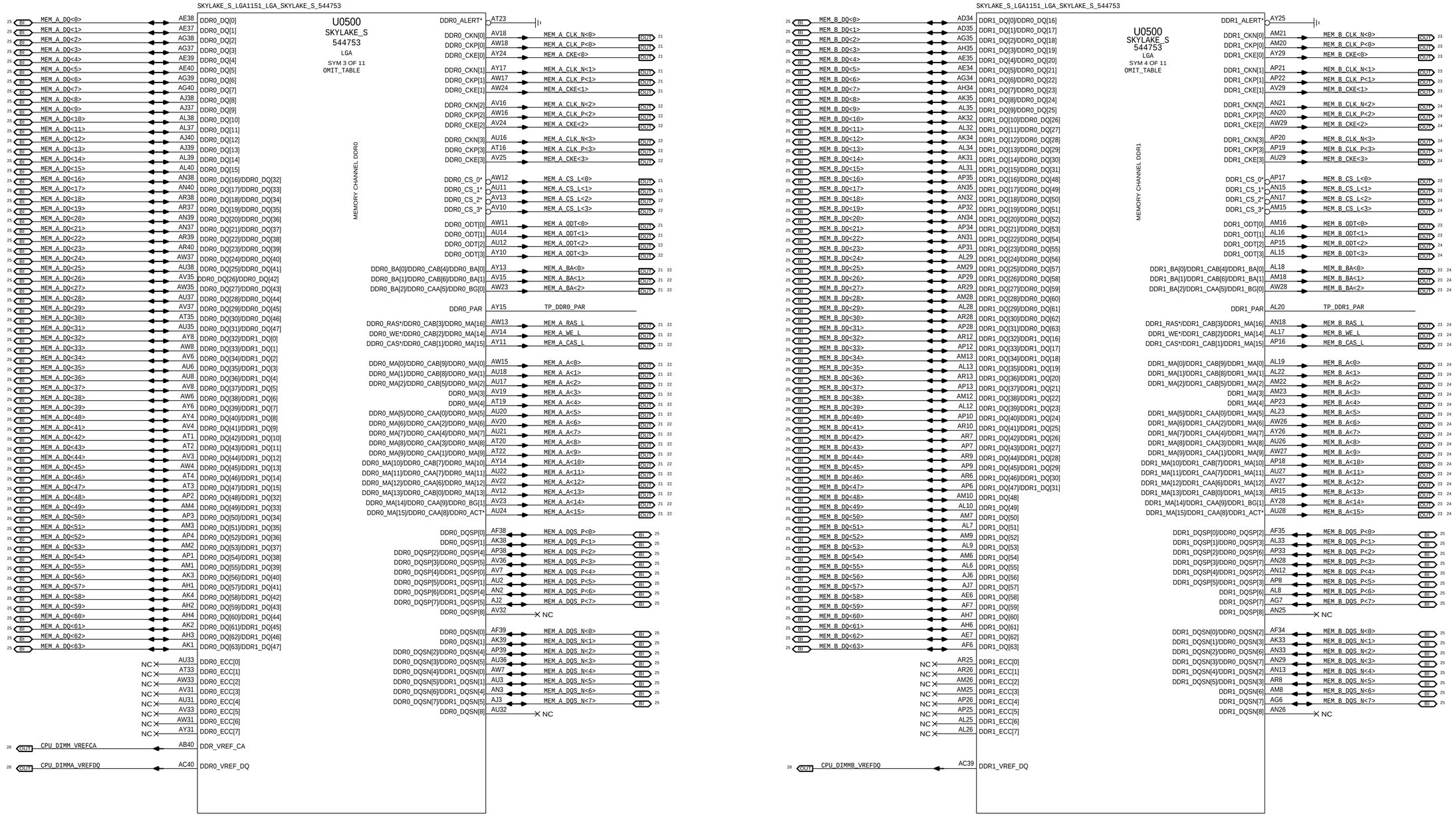

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PAGE TITLE

CPU & CHIPSET: DDR3L Interfaces

Apple Inc.

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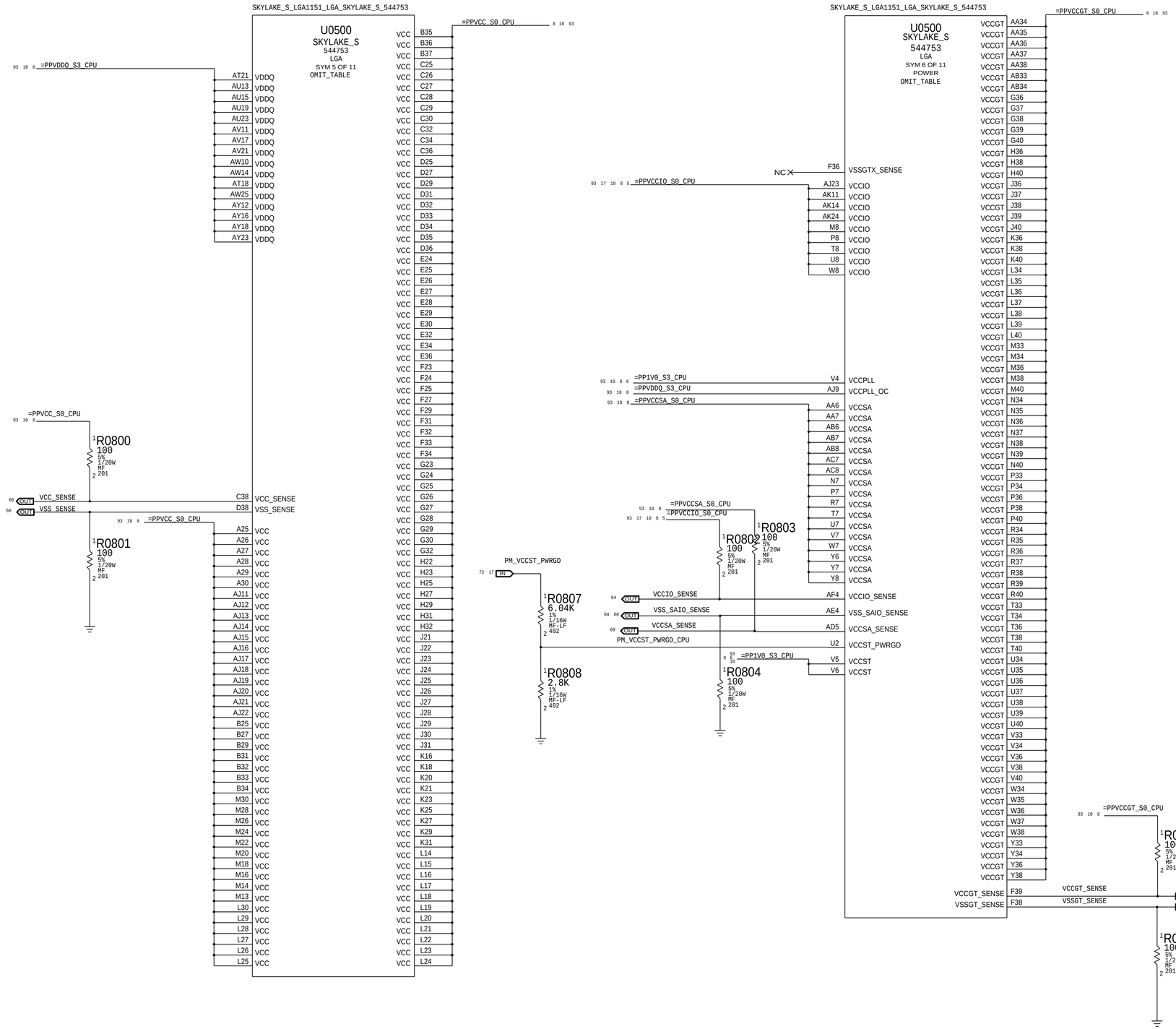

SYNC_MASTER=J78_MLB SYNC_DATE=06/30/2014

PAGE TITLE

CPU & CHIPSET: CPU Power

Apple Inc.

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SKYLAKE_S_LGA1151_LGA_SKYLAKE_S_544753

U0500
SKYLAKE_S
544753
LGA
SYM 7 OF 11
GROUND
OMIT_TABLE

A7	VSS	VSS	AJ35
A11	VSS	VSS	AJ36
A13	VSS	VSS	AK5
A15	VSS	VSS	AK6
A17	VSS	VSS	AK7
A24	VSS	VSS	AK8
AA3	VSS	VSS	AK9
AA8	VSS	VSS	AK10
AA33	VSS	VSS	AK12
AB5	VSS	VSS	AK13
AB39	VSS	VSS	AK15
AC3	VSS	VSS	AK16
AC6	VSS	VSS	AK17
AC33	VSS	VSS	AK18
AC34	VSS	VSS	AK19
AC35	VSS	VSS	AK20
AD1	VSS	VSS	AK23
AD4	VSS	VSS	AK25
AD6	VSS	VSS	AK26
AD7	VSS	VSS	AK28
AD8	VSS	VSS	AK29
AD33	VSS	VSS	AK30
AD36	VSS	VSS	AK36
AD37	VSS	VSS	AK37
AD38	VSS	VSS	AK40
AD39	VSS	VSS	AL1
AD40	VSS	VSS	AL2
AE3	VSS	VSS	AL3
AE5	VSS	VSS	AL4
AE8	VSS	VSS	AL5
AE33	VSS	VSS	AL11
AE36	VSS	VSS	AL14
AF1	VSS	VSS	AL21
AF5	VSS	VSS	AL24
AF8	VSS	VSS	AL27
AF33	VSS	VSS	AL30
AF36	VSS	VSS	AL36
AF37	VSS	VSS	AM5
AF40	VSS	VSS	AM11
AG1	VSS	VSS	AM14
AG2	VSS	VSS	AM17
AG3	VSS	VSS	AM19
AG4	VSS	VSS	AM24
AG5	VSS	VSS	AM27
AG8	VSS	VSS	AM30
AG33	VSS	VSS	AM31
AG36	VSS	VSS	AM32
AH5	VSS	VSS	AM33
AH8	VSS	VSS	AM34
AH33	VSS	VSS	AM35
AH36	VSS	VSS	AM36
AH37	VSS	VSS	AM37
AH38	VSS	VSS	AM38
AH39	VSS	VSS	AM39
AH40	VSS	VSS	AM40
AJ1	VSS	VSS	AN1
AJ4	VSS	VSS	AN4
AJ5	VSS	VSS	AN5
AJ8	VSS	VSS	AN6
AJ31	VSS	VSS	AN7
AJ32	VSS	VSS	AN8
AJ33	VSS	VSS	AN9
AJ34	VSS	VSS	AN10

SKYLAKE_S_LGA1151_LGA_SKYLAKE_S_544753

U0500
SKYLAKE_S
544753
LGA
SYM 8 OF 11
GROUND
OMIT_TABLE

AN11	VSS	VSS	AT32
AN14	VSS	VSS	AT34
AN16	VSS	VSS	AT36
AN19	VSS	VSS	AT37
AN22	VSS	VSS	AT38
AN23	VSS	VSS	AT39
AN24	VSS	VSS	AT40
AN27	VSS	VSS	AU1
AN30	VSS	VSS	AU4
AN36	VSS	VSS	AU5
AP5	VSS	VSS	AU7
AP11	VSS	VSS	AU25
AP14	VSS	VSS	AU30
AP24	VSS	VSS	AU34
AP27	VSS	VSS	AV2
AP30	VSS	VSS	AV5
AP36	VSS	VSS	AV9
AP37	VSS	VSS	AV26
AP40	VSS	VSS	AV28
AR1	VSS	VSS	AV30
AR2	VSS	VSS	AV34
AR3	VSS	VSS	AV38
AR4	VSS	VSS	AW3
AR5	VSS	VSS	AW5
AR11	VSS	VSS	AW9
AR14	VSS	VSS	AW30
AR16	VSS	VSS	AW32
AR17	VSS	VSS	AW34
AR18	VSS	VSS	AW36
AR19	VSS	VSS	AY5
AR20	VSS	VSS	AY7
AR21	VSS	VSS	AY9
AR22	VSS	VSS	AY27
AR23	VSS	VSS	AY30
AR24	VSS	VSS	B6
AR27	VSS	VSS	B24
AR30	VSS	VSS	B26
AR31	VSS	VSS	B28
AR32	VSS	VSS	B30
AR33	VSS	VSS	C5
AR34	VSS	VSS	C8
AR35	VSS	VSS	C10
AR36	VSS	VSS	C12
AT5	VSS	VSS	C14
AT6	VSS	VSS	C16
AT7	VSS	VSS	C18
AT8	VSS	VSS	C20
AT9	VSS	VSS	C22
AT10	VSS	VSS	C24
AT11	VSS	VSS	C31
AT12	VSS	VSS	C33
AT13	VSS	VSS	C35
AT14	VSS	VSS	C37
AT15	VSS	VSS	D4
AT17	VSS	VSS	D7
AT24	VSS	VSS	D24
AT25	VSS	VSS	D26
AT26	VSS	VSS	D28
AT27	VSS	VSS	D30
AT28	VSS	VSS	D37
AT29	VSS	VSS	D39
AT30	VSS	VSS	E3
AT31	VSS	VSS	E6

SKYLAKE_S_LGA1151_LGA_SKYLAKE_S_544753

U0500
SKYLAKE_S
544753
LGA
SYM 9 OF 11
GROUND
OMIT_TABLE

E9	VSS	VSS	K30
E11	VSS	VSS	K33
E13	VSS	VSS	K35
E15	VSS	VSS	K37
E17	VSS	VSS	K39
E19	VSS	VSS	L3
E21	VSS	VSS	L6
E23	VSS	VSS	L9
E31	VSS	VSS	L11
E33	VSS	VSS	L13
E35	VSS	VSS	L32
E37	VSS	VSS	M1
F1	VSS	VSS	M4
F4	VSS	VSS	M7
F7	VSS	VSS	M10
F10	VSS	VSS	M12
F22	VSS	VSS	M15
F26	VSS	VSS	M17
F28	VSS	VSS	M19
F30	VSS	VSS	M21
F40	VSS	VSS	M23
G3	VSS	VSS	M25
G6	VSS	VSS	M27
G11	VSS	VSS	M29
G13	VSS	VSS	M35
G15	VSS	VSS	M37
G17	VSS	VSS	M39
G19	VSS	VSS	N3
G22	VSS	VSS	N6
G31	VSS	VSS	N8
G33	VSS	VSS	N33
H1	VSS	VSS	P1
H4	VSS	VSS	P4
H7	VSS	VSS	P35
H9	VSS	VSS	P37
H21	VSS	VSS	P39
H24	VSS	VSS	R3
H26	VSS	VSS	R6
H28	VSS	VSS	R8
H30	VSS	VSS	R33
H35	VSS	VSS	T1
H37	VSS	VSS	T4
H39	VSS	VSS	T35
J3	VSS	VSS	T37
J6	VSS	VSS	T39
J10	VSS	VSS	U3
J12	VSS	VSS	U6
J16	VSS	VSS	U33
J18	VSS	VSS	V1
J20	VSS	VSS	V8
J32	VSS	VSS	V35
J34	VSS	VSS	V37
K1	VSS	VSS	V39
K4	VSS	VSS	W3
K7	VSS	VSS	W6
K14	VSS	VSS	W33
K15	VSS	VSS	Y5
K17	VSS	VSS	Y35
K19	VSS	VSS	Y37
K22	VSS	VSS	G8
K24	VSS	VSS	H8
K26	VSS	VSS	AY3
K28	VSS		
		VSS_NCTF	A4
		VSS_NCTF	B38
		VSS_NCTF	C2
		VSS_NCTF	D40

SYNC_MASTER=J78_MLB SYNC_DATE=06/30/2014

PAGE TITLE
CPU & CHIPSET: CPU Ground

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DRAWING NUMBER 051-00321
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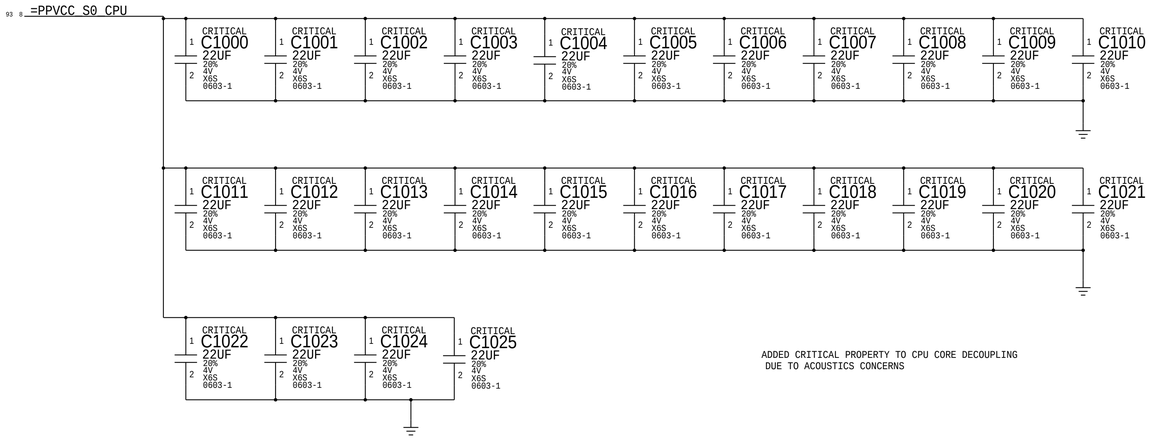
CPU VCORE DECOUPLING

Intel Recommendation:12x 22UF 0805 (top side cavity)
6x 22UF 0603 (top side cavity)
5x 22UF 0805 (top side outside cavity)

Apple Implementation:26x 22UF 0603

Layout Note: These caps should be placed symmetrically on Top and Bottom sides.
BULK CAPS ON CPU VREG PAGE 71



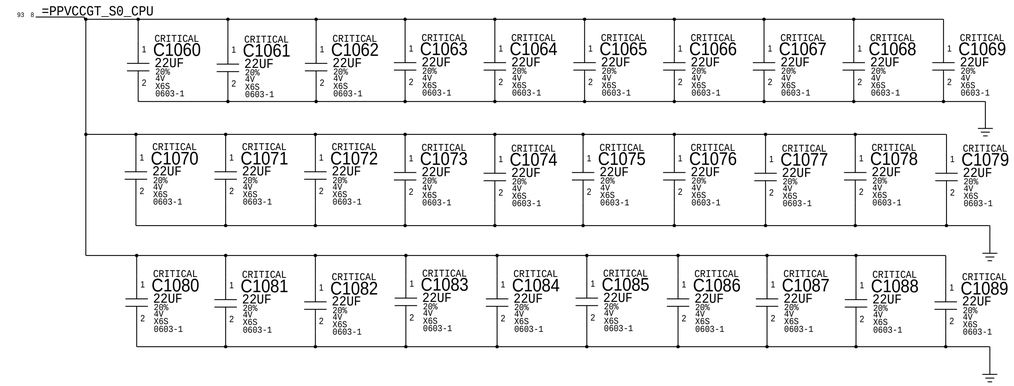
ADDED CRITICAL PROPERTY TO CPU CORE DECOUPLING
DUE TO ACOUSTICS CONCERNS

CPU GT DECOUPLING

Intel Recommendation:9x 47UF 0805 (top side cavity)
4x 47UF 0805 (top side outside cavity)

Apple Implementation: 30x 22uF 0603

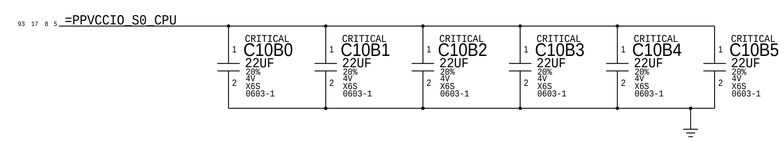
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



CPU VCCIO DECOUPLING

Intel Recommendation:5x 22UF 0603 (top side cavity)
1x 22UF 0805 (top side cavity)

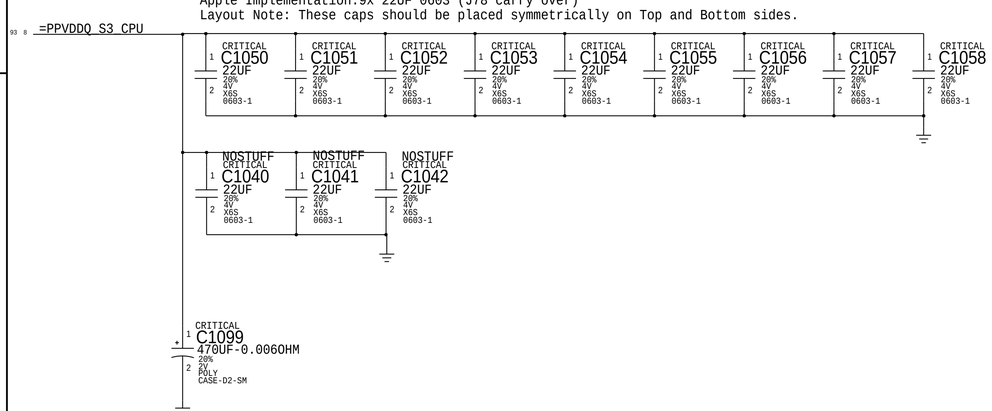
Apple Implementation:(following Intel recommendation w/ 0603)
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



Memory (CPU VCCDDR) DECOUPLING

Intel Recommendation:4x 22UF 0603 (top side outside cavity)

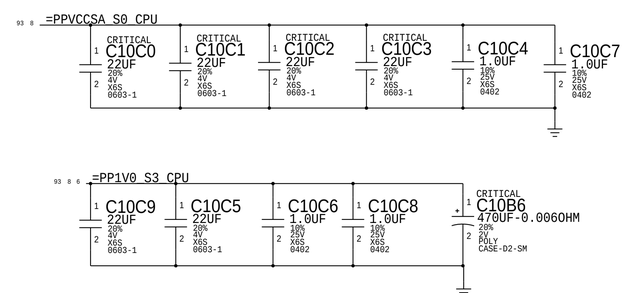
Apple Implementation:9x 22UF 0603 (J78 carry over)
Layout Note: These caps should be placed symmetrically on Top and Bottom sides.



CPU VCCSA / VCCST+VCCPLL DECOUPLING

Intel Recommendation:2x 22UF 0603 near top side cavity

Apple Implementation: VCCST/VCCPLL: 1X 22UF 0603/2X 1UF 0402
Layout Note: These caps should be placed on top side cavity.



SYNC_MASTER=J78_MLB SYNC_DATE=06/30/2014

PAGE TITLE
CPU & CHIPSET: CPU Decoupling

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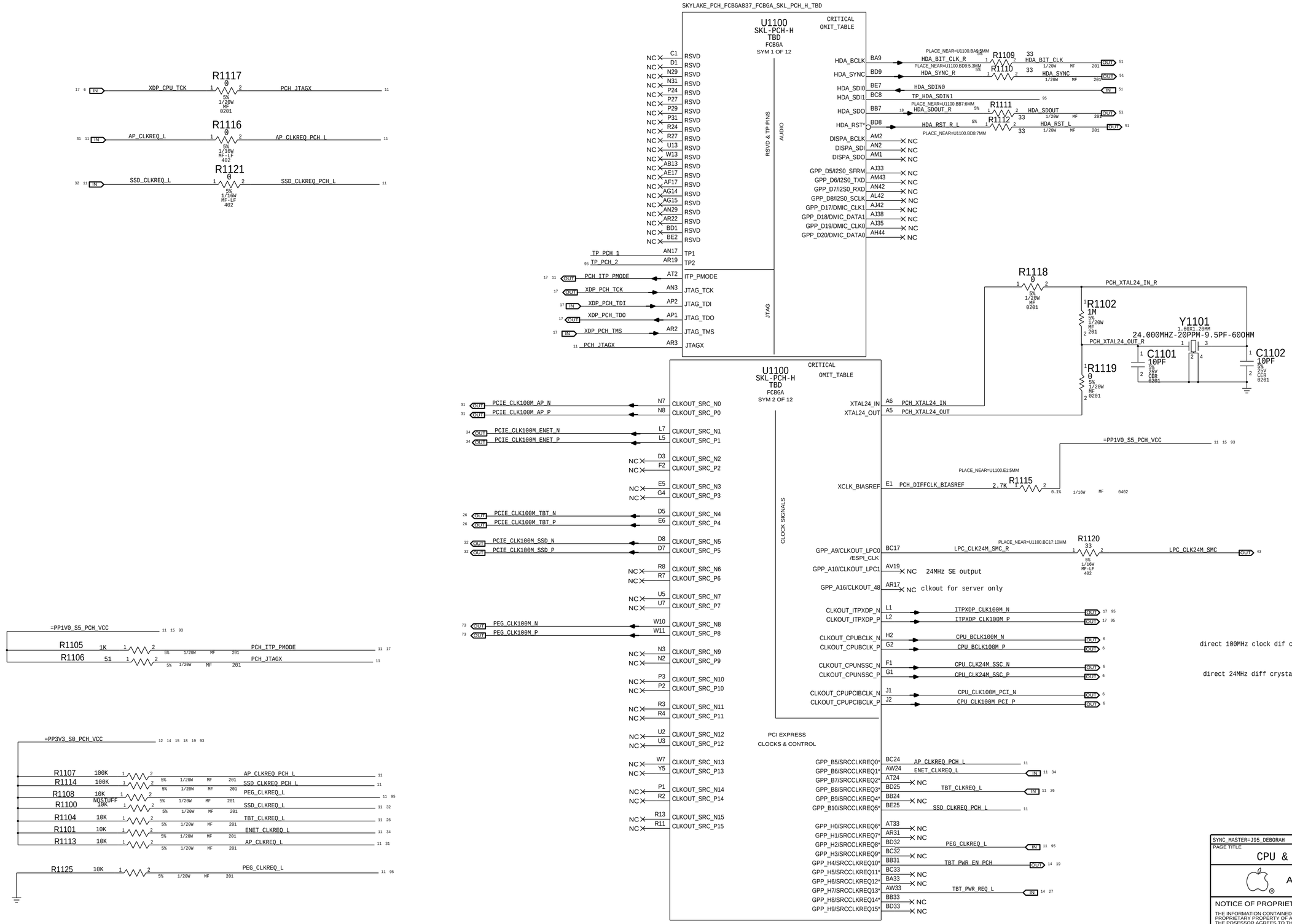

SYNC_MASTER=J95_DEBORAH SYNC_DATE=10/20/2014

PAGE TITLE

CPU & CHIPSET: Clocks/HDA/JTAG

Apple Inc.

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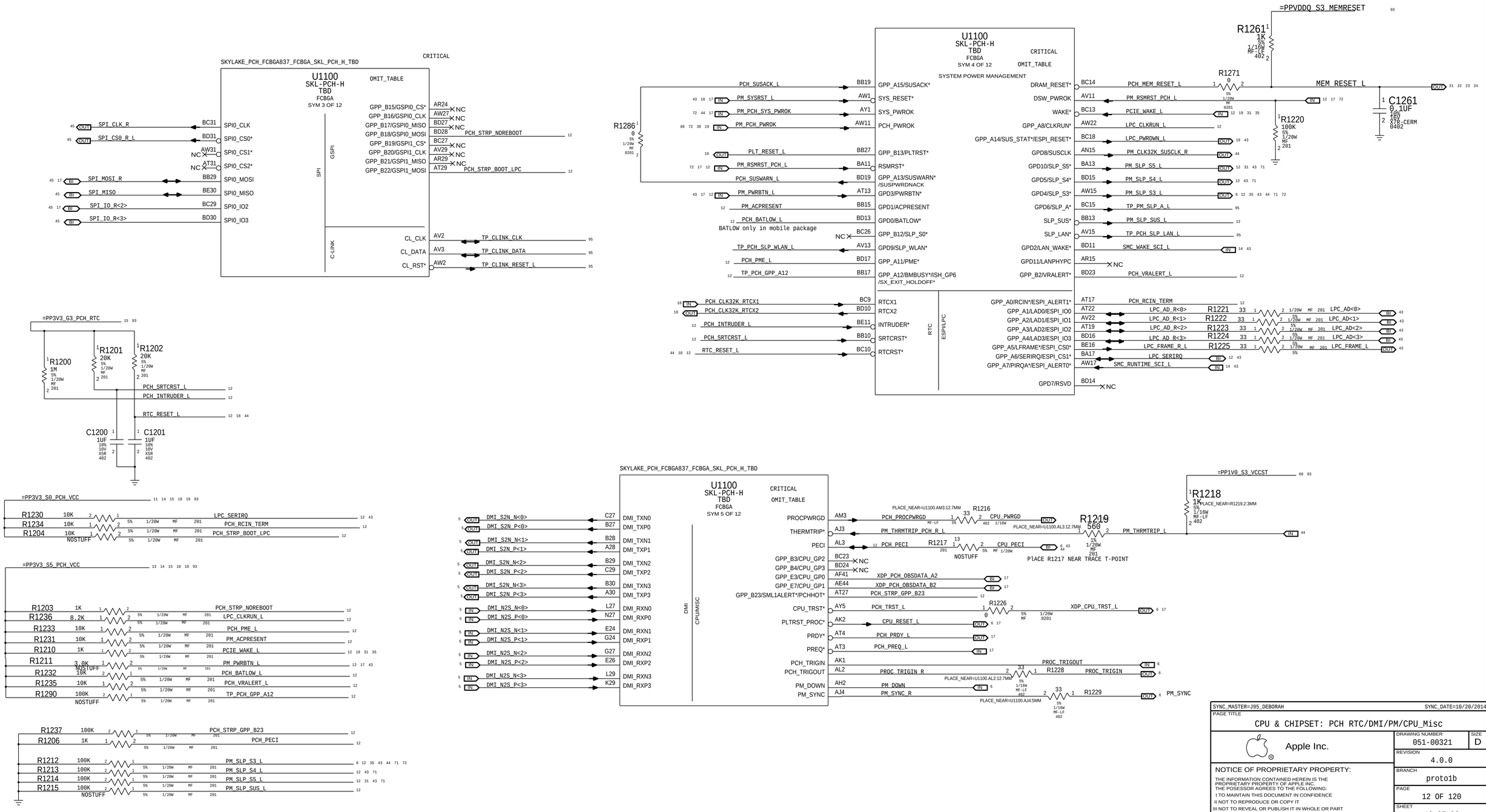

SYNC_MASTER=J95_DEBORAH	SYNC_DATE=10/20/2014
PAGE TITLE	CPU & CHIPSET: PCH RTC/DMI/PM/CPU_Misc
Apple Inc.	DRAWING NUMBER 051-00321 · SIZE D · REVISION 4.0.0 · BRANCH proto1b · PAGE 12 OF 120 · SHEET 12 OF 96

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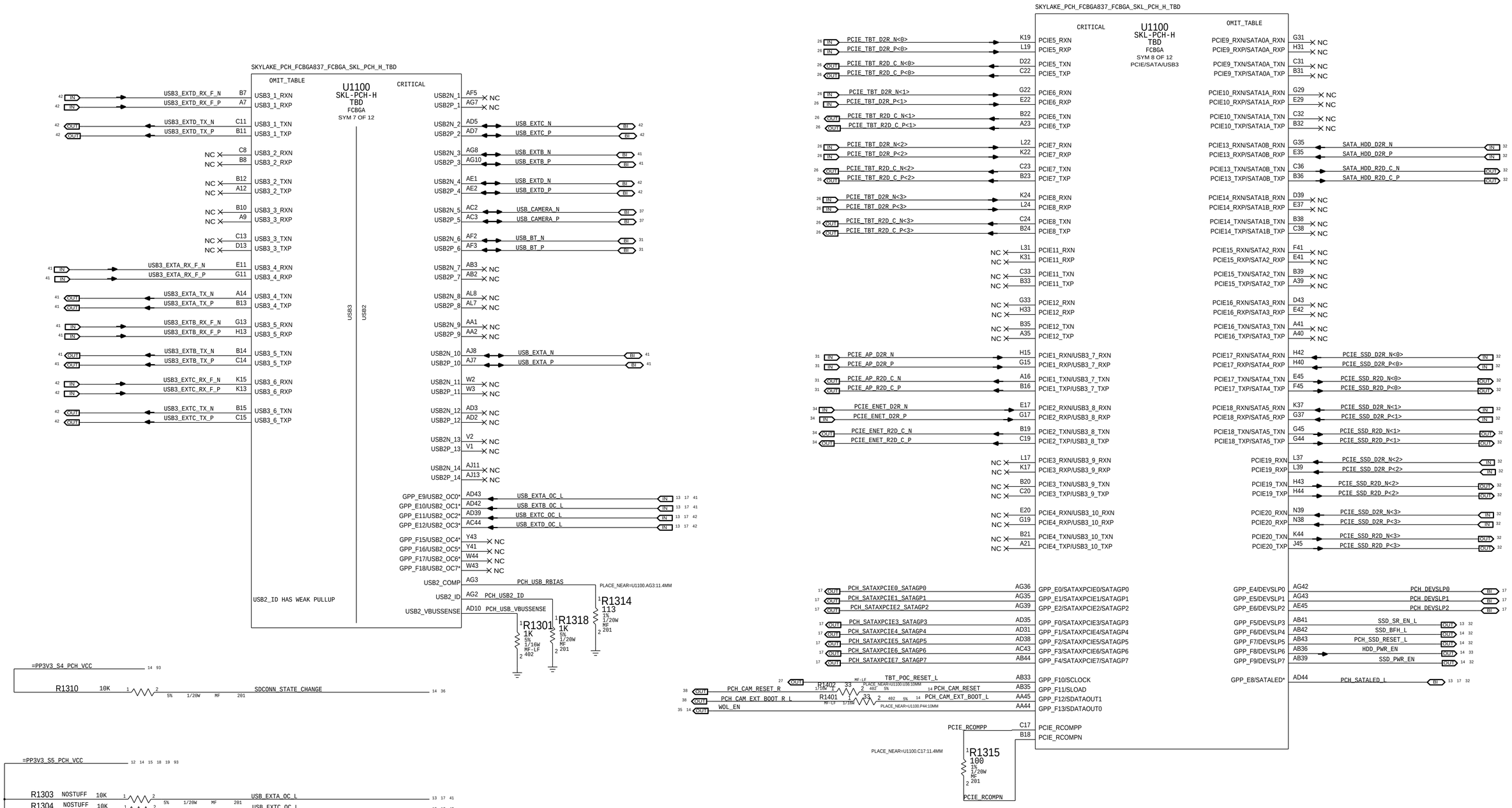

SYNC_MASTER=J95_DEBORAH SYNC_DATE=10/20/2014

PAGE TITLE

CPU & CHIPSET: PCH PCI-E/USB

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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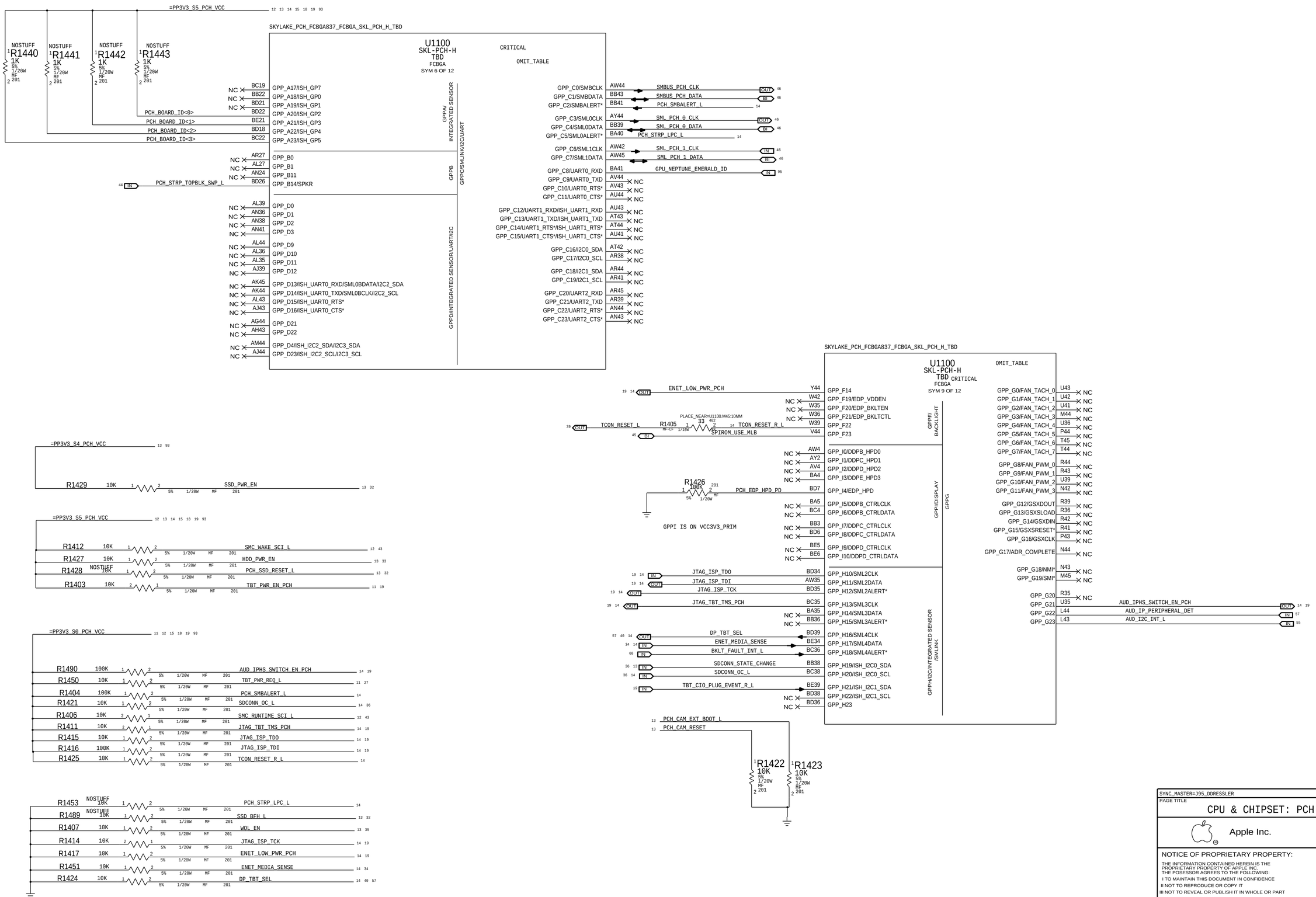

SYNC_MASTER=J95_DDRESSLER SYNC_DATE=02/24/2015

PAGE TITLE

CPU & CHIPSET: PCH GPIO/Misc

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DRAWING NUMBER 051-00321

SIZE D

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BRANCH proto1b

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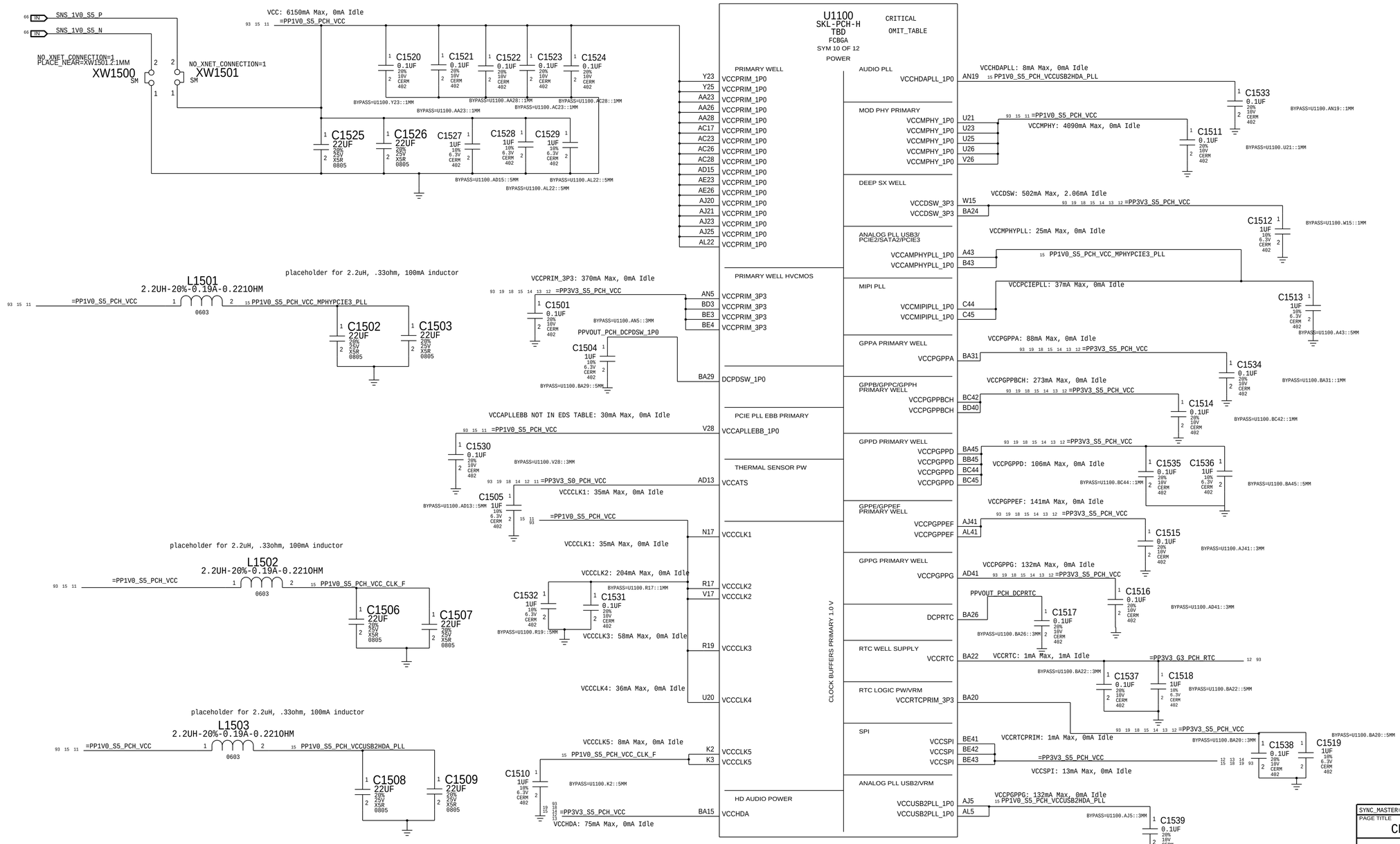
NEED TO ADD 47UF BULK CAPS TO 1.0V AND 3.3V RAIL



Current data from EDS (doc #546717, Rev 0.7).

SYNC_MASTER=J95_DDRESSLER SYNC_DATE=02/24/2015

PAGE TITLE

CPU & CHIPSET: PCH Power/Decoupling

Apple Inc.

DRAWING NUMBER	051-00321
SIZE	D
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BRANCH	proto1b
PAGE	15 OF 120
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SKYLAKE_PCH_FCBGA837_FCBGA_SKL_PCH_H_TBD

U1100
SKL-PCH-H
TBD
FCBGA
SYM 11 OF 12

CRITICAL

OMIT_TABLE

A2	VSS	VSS	M35
A3	VSS	VSS	M42
A4	VSS	VSS	N4
A18	VSS	VSS	N5
A25	VSS	VSS	N10
A32	VSS	VSS	N15
A37	VSS	VSS	N19
A42	VSS	VSS	N22
A44	VSS	VSS	N24
B1	VSS	VSS	N35
B2	VSS	VSS	N36
B3	VSS	VSS	N41
B6	VSS	VSS	P17
B25	VSS	VSS	P19
B37	VSS	VSS	P22
B40	VSS	VSS	P45
B44	VSS	VSS	R5
B45	VSS	VSS	R10
C2	VSS	VSS	R14
C4	VSS	VSS	R22
C10	VSS	VSS	R29
C28	VSS	VSS	R33
C37	VSS	VSS	R38
C42	VSS	VSS	T1
D10	VSS	VSS	T2
D12	VSS	VSS	T4
D15	VSS	VSS	T42
D16	VSS	VSS	U4
D17	VSS	VSS	U8
D19	VSS	VSS	U10
D21	VSS	VSS	U11
D24	VSS	VSS	U14
D25	VSS	VSS	U15
D27	VSS	VSS	U17
D29	VSS	VSS	U18
D30	VSS	VSS	U28
D31	VSS	VSS	U29
D33	VSS	VSS	U31
D35	VSS	VSS	U32
D36	VSS	VSS	U33
D45	VSS	VSS	U38
E13	VSS	VSS	V3
E15	VSS	VSS	V18
E31	VSS	VSS	V20
E33	VSS	VSS	V21
F8	VSS	VSS	V23
F44	VSS	VSS	V25
G9	VSS	VSS	V29
G42	VSS	VSS	V45
H3	VSS	VSS	W4
H17	VSS	VSS	W8
H19	VSS	VSS	W14
H22	VSS	VSS	W31
H24	VSS	VSS	W32
H27	VSS	VSS	W33
H29	VSS	VSS	W38
H35	VSS	VSS	Y17
J3	VSS	VSS	Y18
J5	VSS	VSS	Y20
J7	VSS	VSS	Y21
J10	VSS	VSS	Y26
J11	VSS	VSS	Y28
J39	VSS	VSS	Y29
K4	VSS	VSS	AA4
K10	VSS	VSS	AA17
K27	VSS	VSS	AA18
K33	VSS	VSS	AA20
K36	VSS	VSS	AA21
K42	VSS	VSS	AA25
K43	VSS	VSS	AA29
L4	VSS	VSS	AA42
L8	VSS	VSS	AB4
L12	VSS	VSS	AB5
L13	VSS	VSS	AB7
L15	VSS	VSS	AB8
L41	VSS	VSS	AB10

SKYLAKE_PCH_FCBGA837_FCBGA_SKL_PCH_H_TBD

U1100
SKL-PCH-H
TBD
FCBGA
SYM 12 OF 12

CRITICAL

OMIT_TABLE

AB11	VSS	VSS	AL32
AB14	VSS	VSS	AL33
AB15	VSS	VSS	AL38
AB31	VSS	VSS	AM15
AB32	VSS	VSS	AM17
AB38	VSS	VSS	AM19
AC1	VSS	VSS	AM22
AC18	VSS	VSS	AM24
AC20	VSS	VSS	AM27
AC21	VSS	VSS	AM29
AC25	VSS	VSS	AM45
AC29	VSS	VSS	AN4
AC45	VSS	VSS	AN7
AD4	VSS	VSS	AN8
AD8	VSS	VSS	AN10
AD11	VSS	VSS	AN11
AD14	VSS	VSS	AN22
AD32	VSS	VSS	AN27
AD33	VSS	VSS	AN31
AD36	VSS	VSS	AN39
AE4	VSS	VSS	AP4
AE18	VSS	VSS	AP11
AE20	VSS	VSS	AR5
AE21	VSS	VSS	AR7
AE25	VSS	VSS	AR9
AE28	VSS	VSS	AR33
AE29	VSS	VSS	AR34
AE42	VSS	VSS	AR42
AF18	VSS	VSS	AT9
AF20	VSS	VSS	AT10
AF21	VSS	VSS	AT15
AF23	VSS	VSS	AT36
AF25	VSS	VSS	AU1
AF26	VSS	VSS	AU7
AF28	VSS	VSS	AU35
AF29	VSS	VSS	AU36
AG4	VSS	VSS	AU39
AG11	VSS	VSS	AU45
AG13	VSS	VSS	AV6
AG31	VSS	VSS	AV17
AG32	VSS	VSS	AV24
AG33	VSS	VSS	AV27
AG38	VSS	VSS	AV31
AH1	VSS	VSS	AV33
AH17	VSS	VSS	AW9
AH18	VSS	VSS	AW13
AH20	VSS	VSS	AW19
AH21	VSS	VSS	AW29
AH23	VSS	VSS	AW37
AH25	VSS	VSS	AY38
AH26	VSS	VSS	AY45
AH28	VSS	VSS	BA1
AH29	VSS	VSS	BB1
AH45	VSS	VSS	BB11
AJ10	VSS	VSS	BB16
AJ14	VSS	VSS	BB21
AJ15	VSS	VSS	BB25
AJ17	VSS	VSS	BB30
AJ18	VSS	VSS	BB34
AJ26	VSS	VSS	BC1
AJ28	VSS	VSS	BC2
AJ29	VSS	VSS	BD2
AJ31	VSS	VSS	BD43
AJ32	VSS	VSS	BD44
AJ36	VSS	VSS	BD45
AK4	VSS	VSS	BE9
AK42	VSS	VSS	BE14
AL4	VSS	VSS	BE18
AL10	VSS	VSS	BE23
AL11	VSS	VSS	BE28
AL13	VSS	VSS	BE32
AL17	VSS	VSS	BE37
AL19	VSS	VSS	BE40
AL24	VSS	VSS	BE44
AL29	VSS		

SYNC_MASTER=J95_DEBORAH SYNC_DATE=10/20/2014

PAGE TITLE
CPU & CHIPSET: PCH Grounds

Apple Inc.

DRAWING NUMBER 051-00321
SIZE D
REVISION 4.0.0
BRANCH proto1b
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Primary Micro2-XDP

Extra BPM Testpoints

XDP_BPM_L<2> — TP1802
XDP_BPM_L<3> — TP1803

CRB has no-stuff S3 pull-up on PREQ_L
PDG allows any value from 51 to 3K

Connect Hook2 to CFG<0>
and pull-up to S0
(as in CRB)

WF: SB DPDG says HOOK1 is BP_PWRGD_RST#

NOTE: This is a MERGED XDP: = Primary XDP with CPU & PCH JTAGs in a Dual-Scan-Chain

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

NOTE: This is not the standard XDP pinout,
there is a horizontal mirroring for
use with 921-0133 Adapter Flex to
support chipset debug.

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM
998-2516

ICT CPU & PCH JTAG Test-Points:

TP1840 = TMS
TP1841 = TDI
TP1842 = TDO
TP1843 = TCK0
(TP1844 = TCK1)
TP1845 = DAISY
TP1846 = DAISY_L
TP1847 = TRST_L

NOTE: TDI and TMS are terminated in CPU.

ICT CPU & PCH JTAG Daisy-Chain Support (S0):

To configure CPU and PCH JTAG in an ICT Daisy-Chain:
Drive ICT_JTAG_DAISY to 5V and
drive ICT_JTAG_DAISY_L to Ground.

Secondary (PCH) Micro2-XDP

NOTE: This is not the standard XDP pinout,
there is a horizontal mirroring for
use with 921-0133 Adapter Flex to
support chipset debug.

CRITICAL
XDP_CONN
J1850
DF40RC-60DP-0.4V
M-ST-SM
998-2516

PCH SIGNALS / XDP SIGNALS

PCH SIGNALS			XDP SIGNALS
PCH_PREQ_L	OMIT	R1890	XDP_PCH_PREQ_L
PCH_PRDY_L	OMIT	R1893	XDP_PCH_PRDY_L
PCH_SATAXPCIE0_SATAGP0	OMIT	R1894	XDP_PCH_SATAXPCIE0_SATAGP0
PCH_SATAXPCIE1_SATAGP1	OMIT	R1895	XDP_PCH_SATAXPCIE1_SATAGP1
PCH_SATAXPCIE2_SATAGP2	OMIT	R1880	XDP_PCH_SATAXPCIE2_SATAGP2
PCH_SATAXPCIE3_SATAGP3	OMIT	R1881	XDP_PCH_SATAXPCIE3_SATAGP3
PCH_SATAXPCIE4_SATAGP4	OMIT	R1896	XDP_PCH_SATAXPCIE4_SATAGP4
PCH_SATAXPCIE5_SATAGP5	OMIT	R1897	XDP_PCH_SATAXPCIE5_SATAGP5
PCH_SATAXPCIE6_SATAGP6	OMIT	R1872	XDP_PCH_SATAXPCIE6_SATAGP6
PCH_SATAXPCIE7_SATAGP7	OMIT	R1873	XDP_PCH_SATAXPCIE7_SATAGP7
XDP_PCH_OBSDATA_A2	OMIT	R1874	XDP_PCH_CPU_GP0
PCH_DEVSLP0	OMIT	R1875	XDP_PCH_DEVSLP0
PCH_ITP_PMODE	OMIT	R1878	XDP_PCH_ITP_PMODE
PCH_DEVSLP1	OMIT	R1879	XDP_PCH_DEVSLP1
PCH_DEVSLP2	OMIT	R1882	XDP_PCH_DEVSLP2
XDP_PCH_OBSDATA_B2	OMIT	R1883	XDP_PCH_CPU_GP1
PCH_SATALED_L	OMIT	R1886	XDP_PCH_SATALED_L
PM_RSMRST_PCH_L	OMIT	R1887	XDP_PCH_RSMRST_L
PM_SYSRST_L	OMIT	R1884	XDP_PM_SYSRST_L
USB_EXTA_OC_L	OMIT	R1833	XDP_PCH_USB2_OC0_L
USB_EXTB_OC_L	OMIT	R1835	XDP_PCH_USB2_OC1_L
USB_EXTC_OC_L	OMIT	R1832	XDP_PCH_USB2_OC2_L
USB_EXTD_OC_L	OMIT	R1834	XDP_PCH_USB2_OC3_L

PCH/XDP Signal Isolation Notes:

R187x and R189x should be placed where
signal path needs to split between route
from PCH to J1850 and path to non-XDP
signal destination (to minimize stub).

SYNC_MASTER=J95_ANDREW SYNC_DATE=01/24/2015
PAGE TITLE
CPU & CHIPSET: XDP
Apple Inc.
DRAWING NUMBER 051-00321
SIZE D
REVISION 4.0.0
BRANCH proto1b
PAGE 18 OF 120
SHEET 17 OF 96

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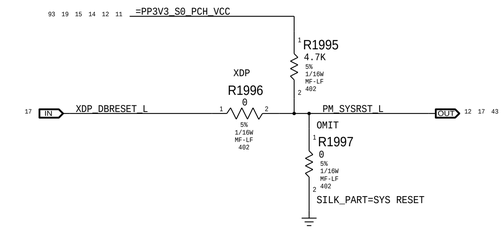
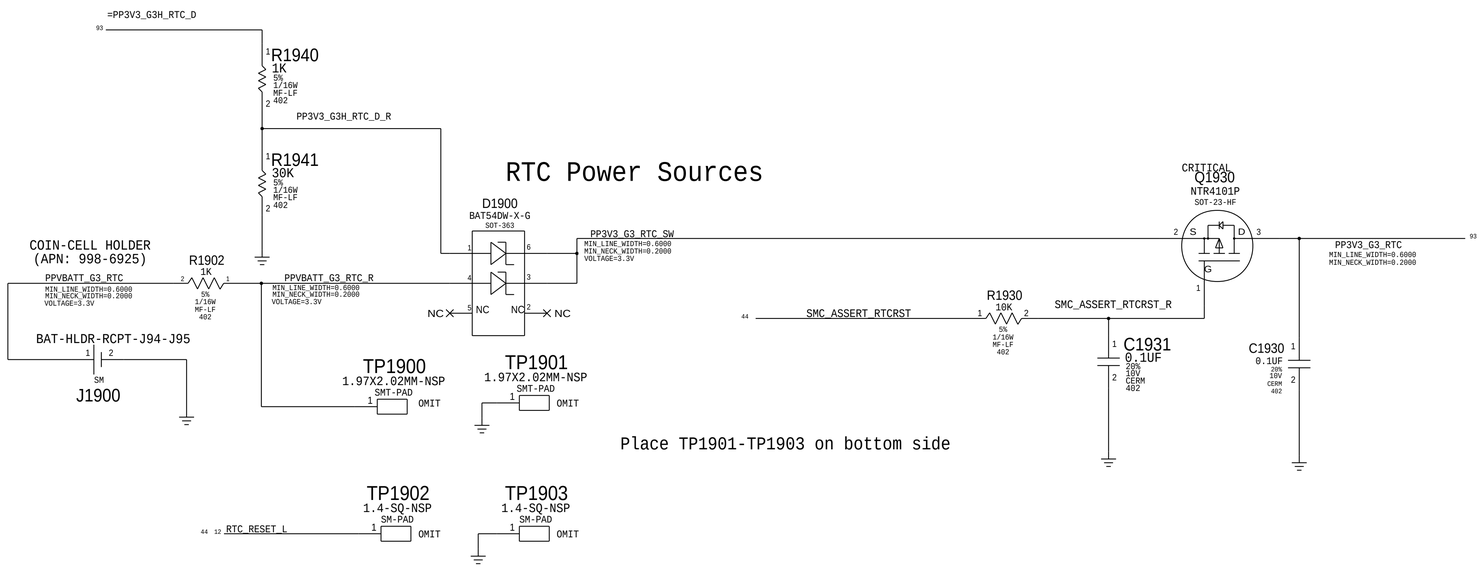
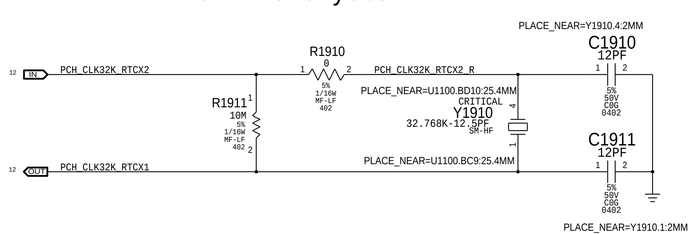
PCH Reset Button



RTC Power Sources

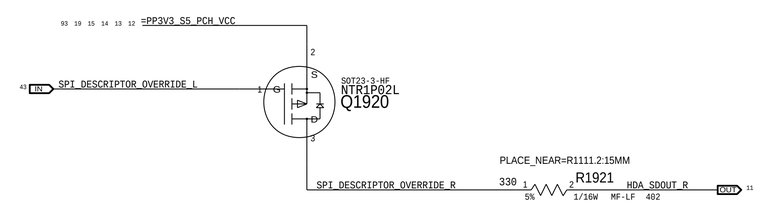


PCH RTC Crystal



PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.



SYNC_MASTER=BRANCH_SYEDKAR	SYNC_DATE=09/10/2014
PAGE TITLE: CPU & CHIPSET: Chipset Support	
Apple Inc.	DRAWING NUMBER: 051-00321 / SIZE: D
	REVISION: 4.0.0
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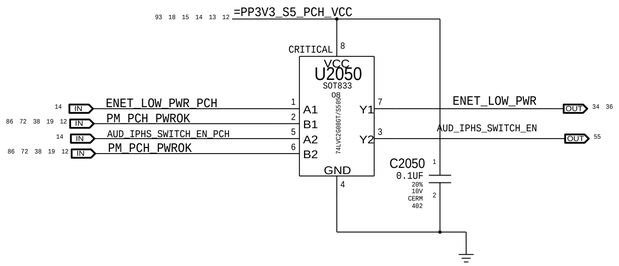
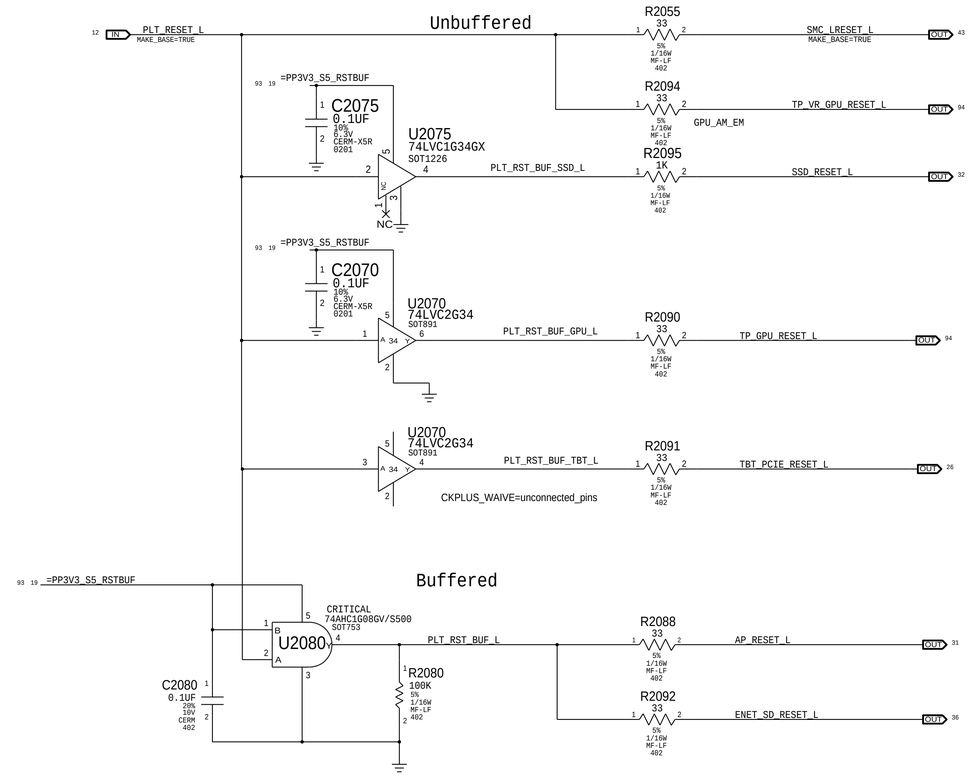
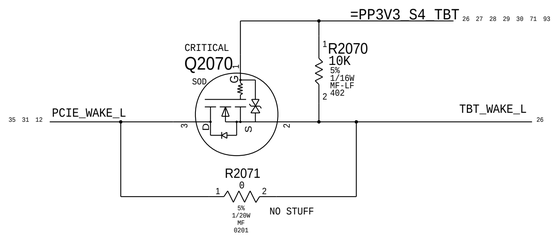
GPIO Glitch Prevention

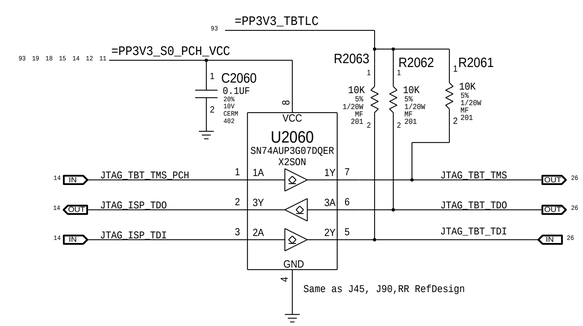


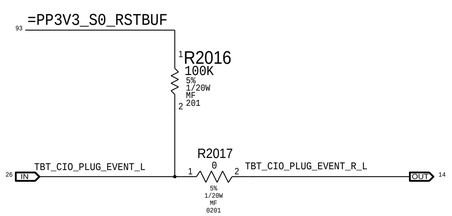
Platform Reset Connections

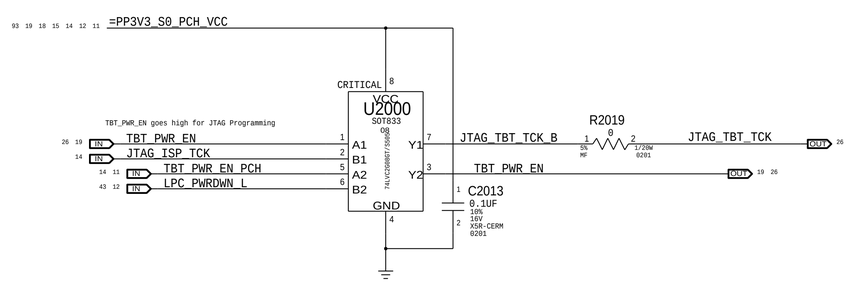




TBT_LC can be on when S0 is off and vice-versa.
Isolation ensure no leakage to FR or PCH
U2060 Supports I/Os powered when VCC = 0V







SYNC_MASTER=J16_IG	SYNC_DATE=04/29/2013
PAGE TITLE	CPU & CHIPSET: Project Chipset Support
Apple Inc.	DRAWING NUMBER 051-00321 SIZE D
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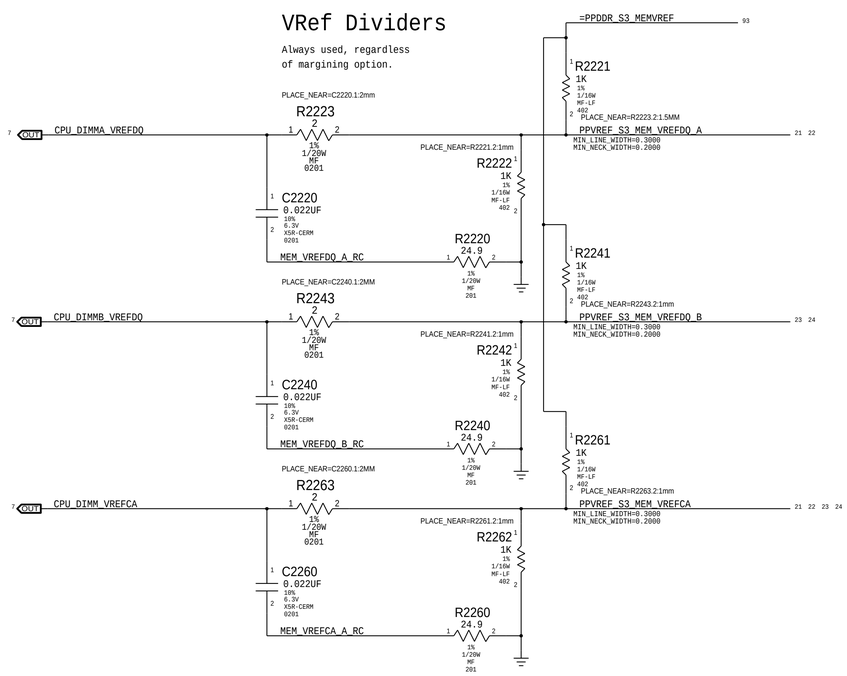

SYNC_MASTER=J78_DAVID SYNC_DATE=03/10/2014

PAGE TITLE

DRAM: VREF/VTT EN

Apple Inc.

DRAWING NUMBER	051-00321
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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

22 20 PPVREF_S3_MEM_VREFDQ_A

C2330 2.2UF 20% 6.3V CERM 402-LF

C2331 0.1UF 20% 10V CERM 402

J2300 SODIMM-P0.60-D8 F-ANG-SM-1 SYM 1 OF 2 CRITICAL

P/N: 516S1019

J2300 SODIMM-P0.60-D8 F-ANG-SM-1 SYM 2 OF 2 MTG HOLE

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

93 22 21 =PPVDDQ_S3_MEM_A

C2310 0.1UF 20% 10V CERM 402
C2311 0.1UF 20% 10V CERM 402
C2312 0.1UF 20% 10V CERM 402
C2313 0.1UF 20% 10V CERM 402
C2314 0.1UF 20% 10V CERM 402
C2315 0.1UF 20% 10V CERM 402
C2316 0.1UF 20% 10V CERM 402
C2317 0.1UF 20% 10V CERM 402

C2300 10UF 20% 6.3V X5R 603
C2301 10UF 20% 6.3V X5R 603
C2318 0.1UF 20% 10V CERM 402
C2319 0.1UF 20% 10V CERM 402
C2320 0.1UF 20% 10V CERM 402
C2321 0.1UF 20% 10V CERM 402
C2322 0.1UF 20% 10V CERM 402
C2323 0.1UF 20% 10V CERM 402

21 MEM_DIMM0_SA<1>
21 MEM_DIMM0_SA<0>
93 22 21 =PP3V3_S0_MEM_A_SPD

C2340 2.2UF 20% 6.3V CERM 402-LF
R2340 10K 5% 1/16W MF-LF 402
R2341 10K 5% 1/16W MF-LF 402

93 22 21 =PPDDRVTT_S0_MEM_A

Pin	Signal	Pin	Signal
1	VREFDQ	2	VSS_0
3	VSS_1	4	DQ4
5	DQ0	6	DQ5
7	DQ1	8	VSS_2
9	VSS_3	10	DQS0*
11	DM0	12	DQS0
13	VSS_4	14	VSS_5
15	DQ2	16	DQ6
17	DQ3	18	DQ7
19	VSS_6	20	VSS_7
21	DQ8	22	DQ12
23	DQ9	24	DQ13
25	VSS_8	26	VSS_9
27	DQS1*	28	DM1
29	DQS1	30	RESET*
31	VSS_10	32	VSS_11
33	DQ10	34	DQ14
35	DQ11	36	DQ15
37	VSS_12	38	VSS_13
39	DQ16	40	DQ20
41	DQ17	42	DQ21
43	VSS_14	44	VSS_15
45	DQS2*	46	DM2
47	DQS2	48	VSS_16
49	VSS_17	50	DQ22
51	DQ18	52	DQ23
53	DQ19	54	VSS_18
55	VSS_19	56	DQ28
57	DQ24	58	DQ29
59	DQ25	60	VSS_20
61	VSS_21	62	DQS3*
63	DM3	64	DQS3
65	VSS_22	66	VSS_23
67	DQ26	68	DQ30
69	DQ27	70	DQ31
71	VSS_24	72	VSS_25
73	CKE0	74	CKE1
75	VDD_0	76	VDD_1
77	NC_0	78	A15
79	BA2	80	A14
81	VDD_2	82	VDD_3
83	A12/BC*	84	A11
85	A9	86	A7
87	VDD_4	88	VDD_5
89	A8	90	A6
91	A5	92	A4
93	VDD_6	94	VDD_7
95	A3	96	A2
97	A1	98	A0
99	VDD_8	100	VDD_9
101	CK0	102	CK1
103	CK0*	104	CK1*
105	VDD_10	106	VDD_11
107	A10_AP	108	BA1
109	BA0	110	RAS*
111	VDD_12	112	VDD_13
113	WE*	114	S0*
115	CAS*	116	ODT0
117	VDD_14	118	VDD_15
119	A13	120	ODT1
121	S1*	122	NC_1
123	VDD_16	124	VDD_17
125	TEST	126	VREFCA
127	VSS_26	128	VSS_27
129	DQ32	130	DQ36
131	DQ33	132	DQ37
133	VSS_28	134	VSS_29
135	DQS4*	136	DM4
137	DQS4	138	VSS_30
139	VSS_31	140	DQ38
141	DQ34	142	DQ39
143	DQ35	144	VSS_32
145	VSS_33	146	DQ44
147	DQ40	148	DQ45
149	DQ41	150	VSS_34
151	VSS_35	152	DQS5*
153	DM5	154	DQS5
155	VSS_36	156	VSS_37
157	DQ42	158	DQ46
159	DQ43	160	DQ47
161	VSS_38	162	VSS_39
163	DQ48	164	DQ52
165	DQ49	166	DQ53
167	VSS_40	168	VSS_41
169	DQS6*	170	DM6
171	DQS6	172	VSS_42
173	VSS_43	174	DQ54
175	DQ50	176	DQ55
177	DQ51	178	VSS_44
179	VSS_45	180	DQ60
181	DQ56	182	DQ61
183	DQ57	184	VSS_46
185	VSS_47	186	DQS7*
187	DM7	188	DQS7
189	VSS_48	190	VSS_49
191	DQ58	192	DQ62
193	DQ59	194	DQ63
195	VSS_50	196	VSS_51
197	SA0	198	EVENT*
199	VDDSPD	200	SDA
201	SA1	202	SCL
203	VTT_0	204	VTT_1

Signal	Pin
=MEM_A_DQ<0>	25 22 BI
=MEM_A_DQ<1>	25 22 BI
=MEM_A_DQ<2>	25 22 BI
=MEM_A_DQ<3>	25 22 BI
=MEM_A_DQ<8>	25 22 BI
=MEM_A_DQ<9>	25 22 BI
=MEM_A_DQS_N<1>	25 22 BI
=MEM_A_DQS_P<1>	25 22 BI
=MEM_A_DQ<10>	25 22 BI
=MEM_A_DQ<11>	25 22 BI
=MEM_A_DQ<16>	25 22 BI
=MEM_A_DQ<17>	25 22 BI
=MEM_A_DQS_N<2>	25 22 BI
=MEM_A_DQS_P<2>	25 22 BI
=MEM_A_DQ<18>	25 22 BI
=MEM_A_DQ<19>	25 22 BI
=MEM_A_DQ<24>	25 22 BI
=MEM_A_DQ<25>	25 22 BI
=MEM_A_DQ<26>	25 22 BI
=MEM_A_DQ<27>	25 22 BI
MEM_A_CKE<0>	7 IN
MEM_A_BA<2>	22 7 IN
MEM_A_A<12>	22 7 IN
MEM_A_A<9>	22 7 IN
MEM_A_A<8>	22 7 IN
MEM_A_A<5>	22 7 IN
MEM_A_A<3>	22 7 IN
MEM_A_A<1>	22 7 IN
MEM_A_CLK_P<0>	7 IN
MEM_A_CLK_N<0>	7 IN
MEM_A_A<10>	22 7 IN
MEM_A_BA<0>	22 7 IN
MEM_A_WE_L	22 7 IN
MEM_A_CAS_L	22 7 IN
MEM_A_A<13>	22 7 IN
MEM_A_CS_L<1>	7 IN
=MEM_A_DQ<32>	25 22 BI
=MEM_A_DQ<33>	25 22 BI
=MEM_A_DQS_N<4>	25 22 BI
=MEM_A_DQS_P<4>	25 22 BI
=MEM_A_DQ<34>	25 22 BI
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=MEM_A_DQ<40>	25 22 BI
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=MEM_A_DQ<42>	25 22 BI
=MEM_A_DQ<43>	25 22 BI
=MEM_A_DQ<48>	25 22 BI
=MEM_A_DQ<49>	25 22 BI
=MEM_A_DQS_N<6>	25 22 BI
=MEM_A_DQS_P<6>	25 22 BI
=MEM_A_DQ<50>	25 22 BI
=MEM_A_DQ<51>	25 22 BI
=MEM_A_DQ<56>	25 22 BI
=MEM_A_DQ<57>	25 22 BI
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=MEM_A_DQ<59>	25 22 BI
MEM_DIMM0_SA<0>	21
=PP3V3_S0_MEM_A_SPD	93 22 21
MEM_DIMM0_SA<1>	21
=MEM_A_DQ<4>	25 22 BI
=MEM_A_DQ<5>	25 22 BI
=MEM_A_DQS_N<0>	25 22 BI
=MEM_A_DQS_P<0>	25 22 BI
=MEM_A_DQ<6>	25 22 BI
=MEM_A_DQ<7>	25 22 BI
=MEM_A_DQ<12>	25 22 BI
=MEM_A_DQ<13>	25 22 BI
MEM_RESET_L	12 22 23 24 IN
=MEM_A_DQ<14>	25 22 BI
=MEM_A_DQ<15>	25 22 BI
=MEM_A_DQ<20>	25 22 BI
=MEM_A_DQ<21>	25 22 BI
=MEM_A_DQ<22>	25 22 BI
=MEM_A_DQ<23>	25 22 BI
=MEM_A_DQ<28>	25 22 BI
=MEM_A_DQ<29>	25 22 BI
=MEM_A_DQS_N<3>	25 22 BI
=MEM_A_DQS_P<3>	25 22 BI
=MEM_A_DQ<30>	25 22 BI
=MEM_A_DQ<31>	25 22 BI
MEM_A_CKE<1>	7 IN
MEM_A_A<15>	22 7 IN
MEM_A_A<14>	22 7 IN
MEM_A_A<11>	22 7 IN
MEM_A_A<7>	22 7 IN
MEM_A_A<6>	22 7 IN
MEM_A_A<4>	22 7 IN
MEM_A_A<2>	22 7 IN
MEM_A_A<0>	22 7 IN
MEM_A_CLK_P<1>	7 IN
MEM_A_CLK_N<1>	7 IN
MEM_A_BA<1>	22 7 IN
MEM_A_RAS_L	22 7 IN
MEM_A_CS_L<0>	7 IN
MEM_A_ODT<0>	7 IN
MEM_A_ODT<1>	7 IN
MEM_EVENT_L	22 23 24 43 44 OUT
=I2C_SODIMMA_SDA	22 46 BI
=I2C_SODIMMA_SCL	22 46 IN
=MEM_A_DQ<36>	25 22 BI
=MEM_A_DQ<37>	25 22 BI
=MEM_A_DQ<38>	25 22 BI
=MEM_A_DQ<39>	25 22 BI
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=MEM_A_DQ<45>	25 22 BI
=MEM_A_DQS_N<5>	25 22 BI
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=MEM_A_DQ<46>	25 22 BI
=MEM_A_DQ<47>	25 22 BI
=MEM_A_DQ<52>	25 22 BI
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=MEM_A_DQ<61>	25 22 BI
=MEM_A_DQS_N<7>	25 22 BI
=MEM_A_DQS_P<7>	25 22 BI
=MEM_A_DQ<62>	25 22 BI
=MEM_A_DQ<63>	25 22 BI

=PPVDDQ_S3_MEM_A 21 22 93

PPVREF_S3_MEM_VREFCA 20 22 23 24

C2335 2.2UF 20% 6.3V CERM 402-LF

C2336 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_A 21 22 93

C2350 1UF 10% 10V X5R 402
C2351 1UF 10% 10V X5R 402
C2352 1UF 10% 10V X5R 402
C2353 1UF 10% 10V X5R 402

SYNC_MASTER=J78_NAT SYNC_DATE=10/30/2013

PAGE TITLE
DRAM: SO-DIMM Connector A Slot0

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DRAWING NUMBER 051-00321 SIZE D
REVISION 4.0.0
BRANCH proto1b
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SHEET 21 OF 96

Page Notes

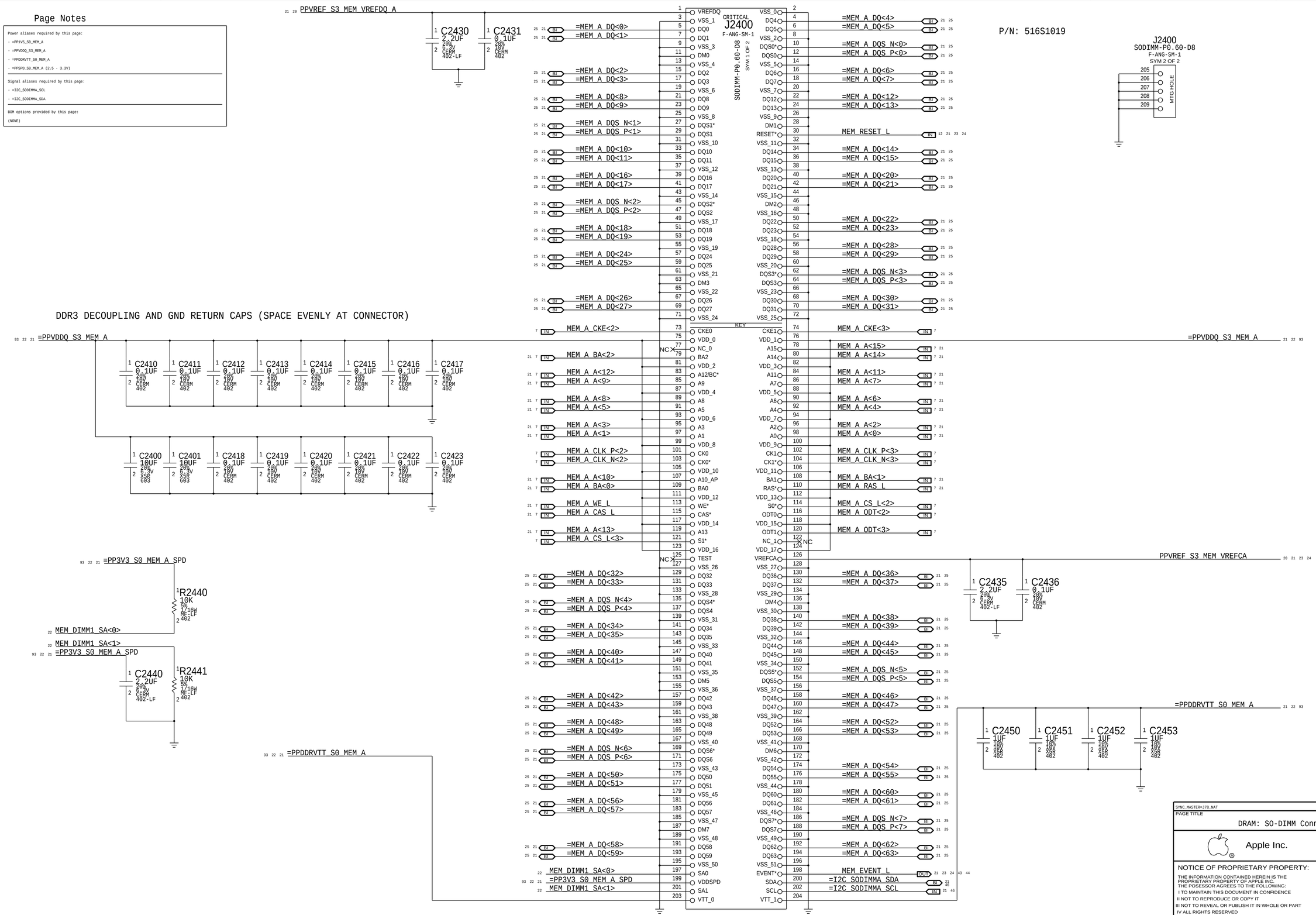
Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1019

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)



SYNC_MASTER=J78_NAT SYNC_DATE=10/30/2013

PAGE TITLE: DRAM: SO-DIMM Connector A Slot1

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DRAWING NUMBER	051-00321
SIZE	D
REVISION	4.0.0
BRANCH	proto1b
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Page Notes

Power aliases required by this page:

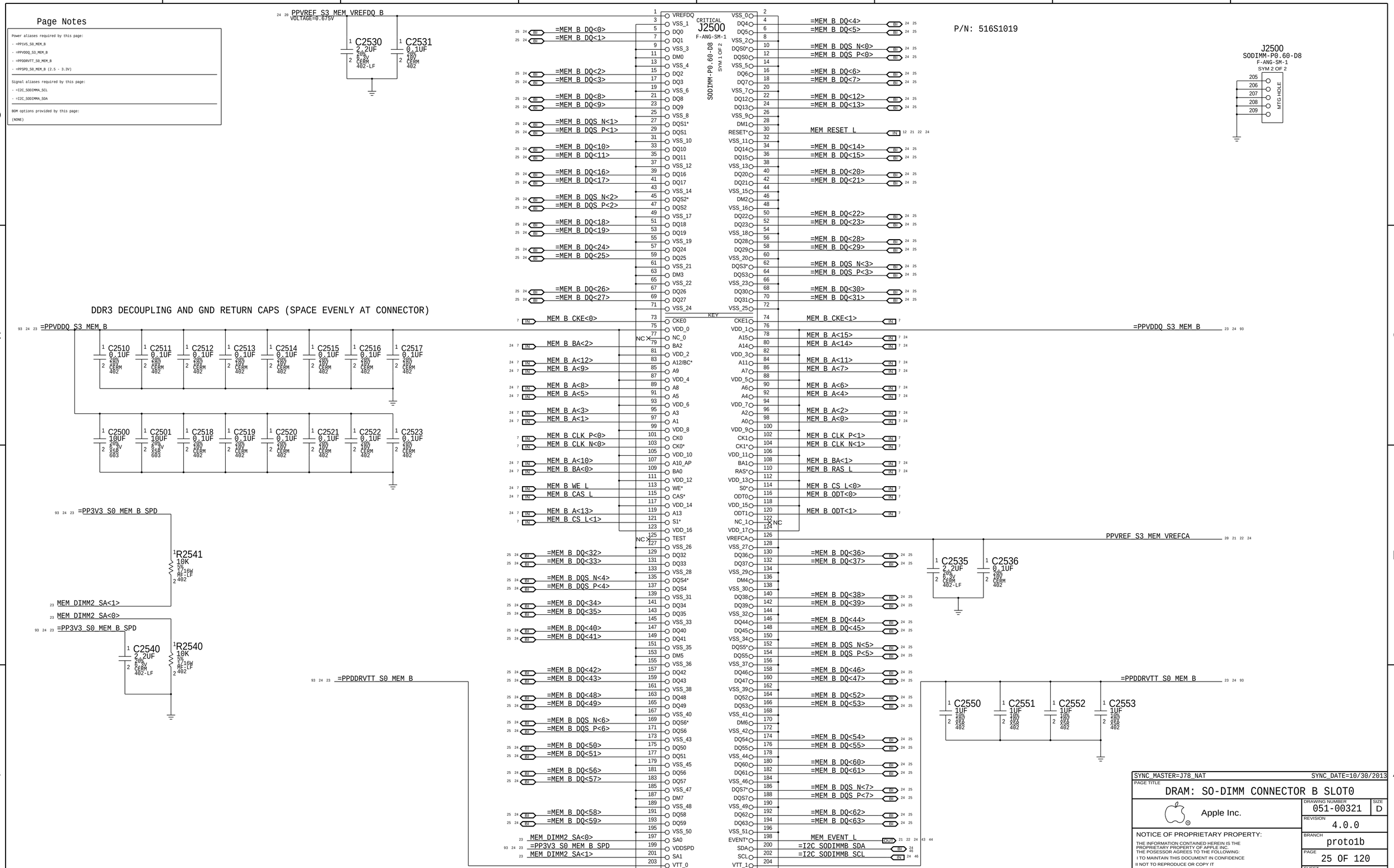
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPODRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)



SYNC_MASTER=J78_NAT SYNC_DATE=10/30/2013

PAGE TITLE

DRAM: SO-DIMM CONNECTOR B SLOT0

Apple Inc.

DRAWING NUMBER	051-00321
SIZE	D
REVISION	4.0.0
BRANCH	proto1b
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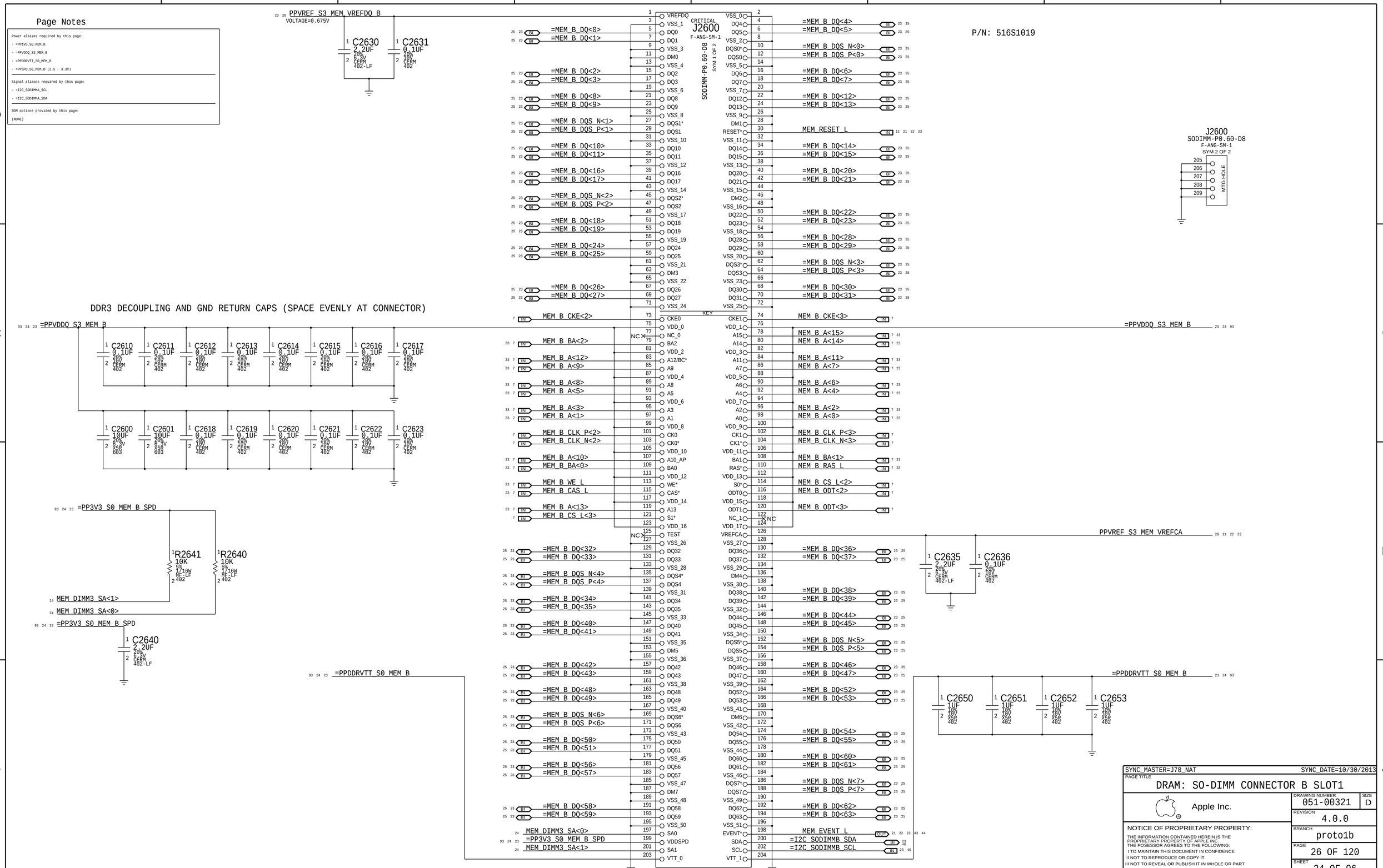
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)



SYNC_MASTER=J78_NAT SYNC_DATE=10/30/2013

PAGE TITLE
DRAM: SO-DIMM CONNECTOR B SLOT1

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D
REVISION 4.0.0
BRANCH proto1b
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THERE ARE NO PIN SWAPS

7	MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	21 22	7	MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	23 24
7	MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	21 22	7	MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	23 24
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7	MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	21 22	7	MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	23 24
7	MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	21 22	7	MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<32>	23 24
7	MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	21 22	7	MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	23 24
7	MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	21 22	7	MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	23 24
7	MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	21 22	7	MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	23 24
7	MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	21 22	7	MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	23 24
7	MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	21 22	7	MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	23 24
7	MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	21 22	7	MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	23 24
7	MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	21 22	7	MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	23 24
7	MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	21 22	7	MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	23 24
7	MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	21 22	7	MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	23 24
7	MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	21 22	7	MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	23 24
7	MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	21 22	7	MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>	23 24
7	MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	21 22	7	MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>	23 24
7	MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	21 22	7	MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	23 24
7	MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	21 22	7	MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	23 24
7	MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	21 22	7	MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	23 24
7	MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	21 22	7	MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	23 24
7	MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	21 22	7	MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	23 24
7	MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	21 22	7	MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	23 24
7	MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	21 22	7	MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	23 24
7	MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	21 22	7	MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	23 24
7	MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	21 22	7	MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	23 24
7	MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	21 22	7	MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	23 24
7	MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	21 22	7	MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	23 24
7	MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	21 22	7	MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	23 24
7	MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	21 22	7	MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	23 24
7	MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	21 22	7	MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	23 24
7	MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	21 22	7	MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	23 24
7	MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	21 22	7	MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	23 24
7	MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	21 22	7	MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	23 24
7	MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	21 22	7	MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	23 24

SYNC_MASTER=J16_IG SYNC_DATE=04/29/2013

PAGE TITLE
DRAM: ALIASES AND BITSWAPS

Apple Inc.

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REVISION 4.0.0
BRANCH proto1b
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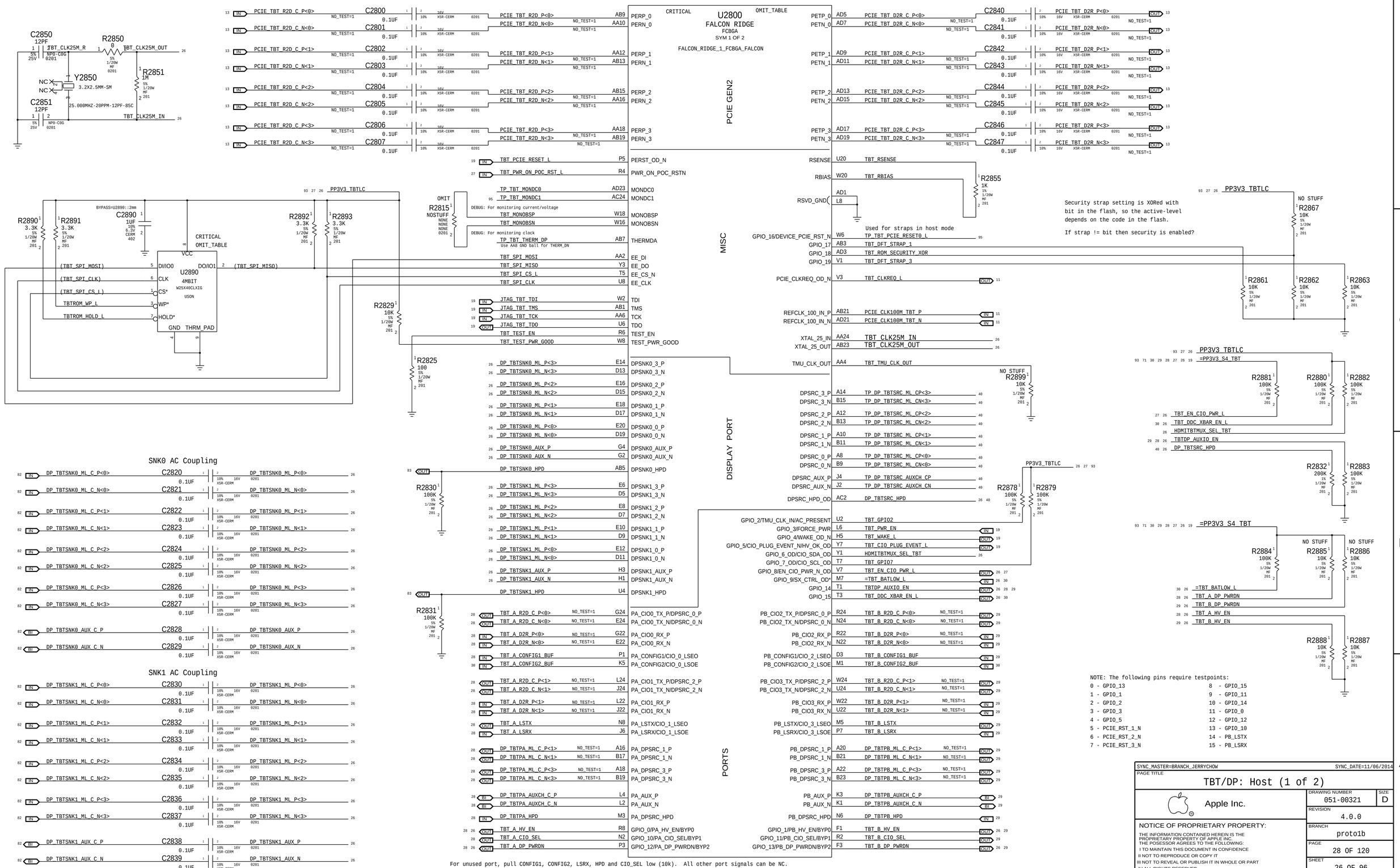
U2800
FALCON RIDGE
FCBGA
SYM 1 OF 2
FALCON_RIDGE_1_FCBGA_FALCON
CRITICAL
OMIT_TABLE
PCIE GEN2
MISC
DISPLAY PORT
PORTS
U2890
4MBIT
W25X40CLXIG
USON
Y2850
3.2X2.5MM-SM
25.000MHZ-20PPM-12PF-85C
SNK0 AC Coupling
SNK1 AC Coupling
Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.
If strap != bit then security is enabled?
Used for straps in host mode
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=BRANCH_JERRYCHOW
SYNC_DATE=11/06/2014
PAGE TITLE
TBT/DP: Host (1 of 2)
Apple Inc.
DRAWING NUMBER
051-00321
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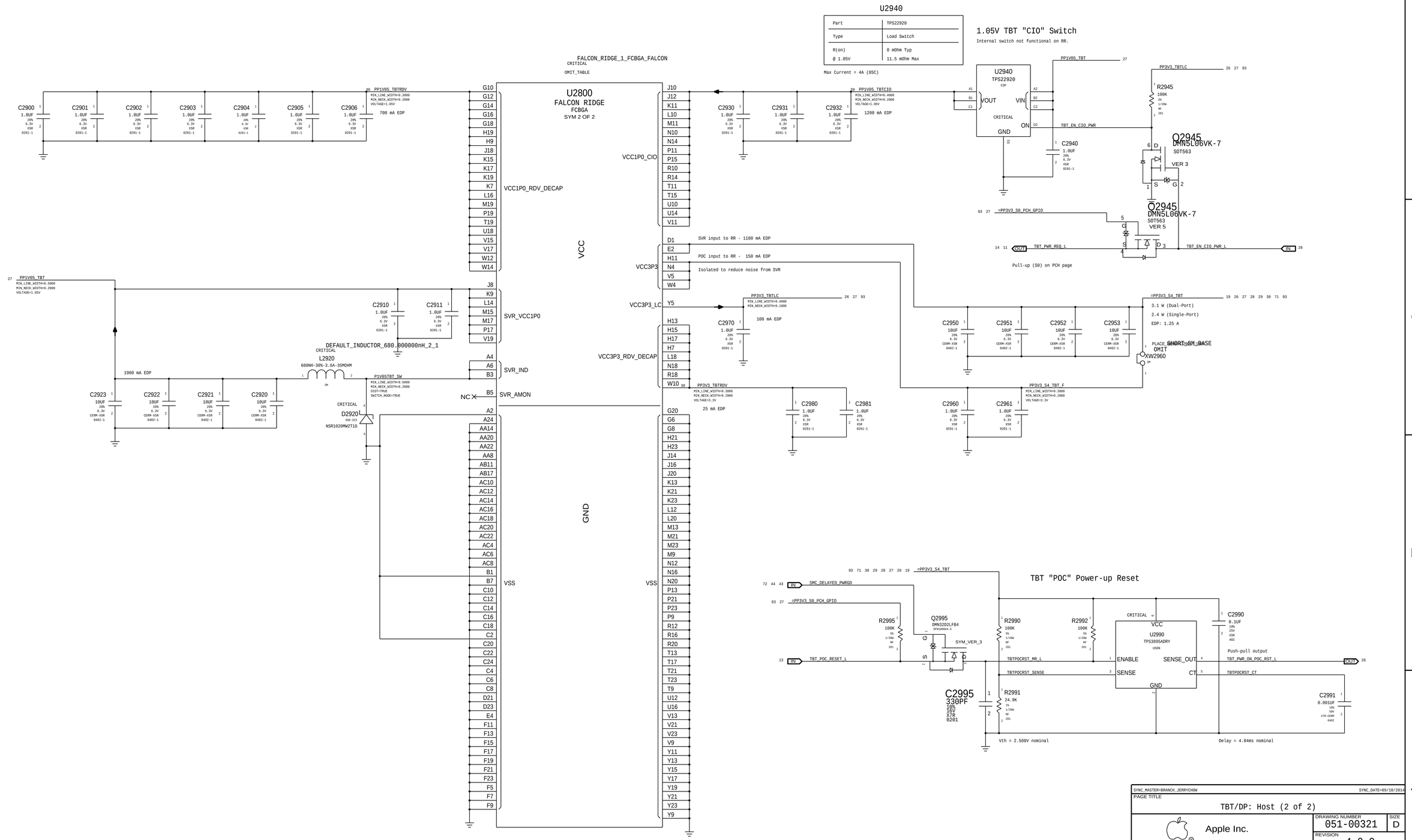

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC_MASTER=BRANCH_JERRYCHOW SYNC_DATE=09/10/2014

PAGE TITLE

TBT/DP: Host (2 of 2)

Apple Inc.

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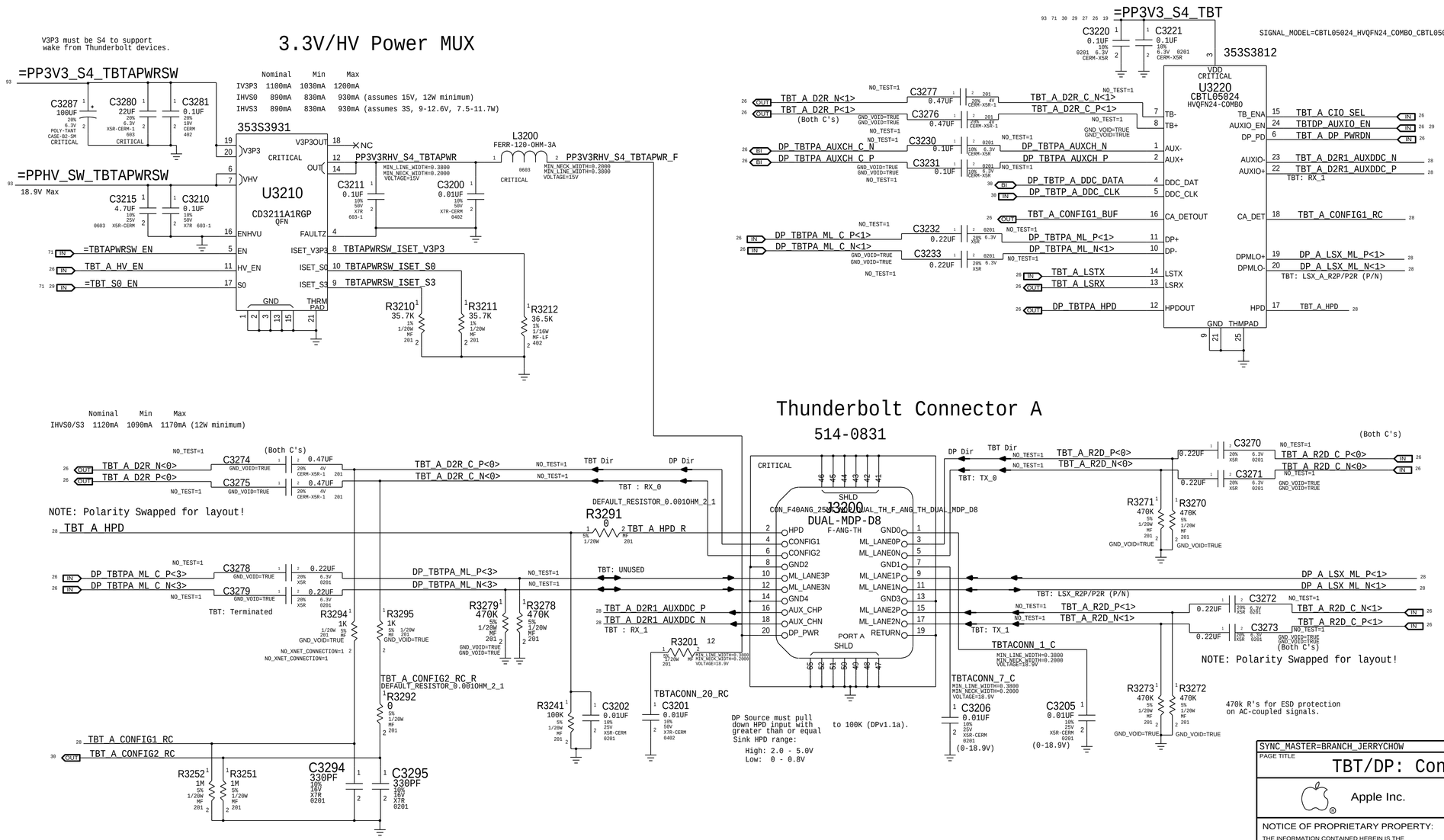

SYNC_MASTER=BRANCH_JERRYCHOW SYNC_DATE=09/10/2014

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TBT/DP: Connector A

Apple Inc.

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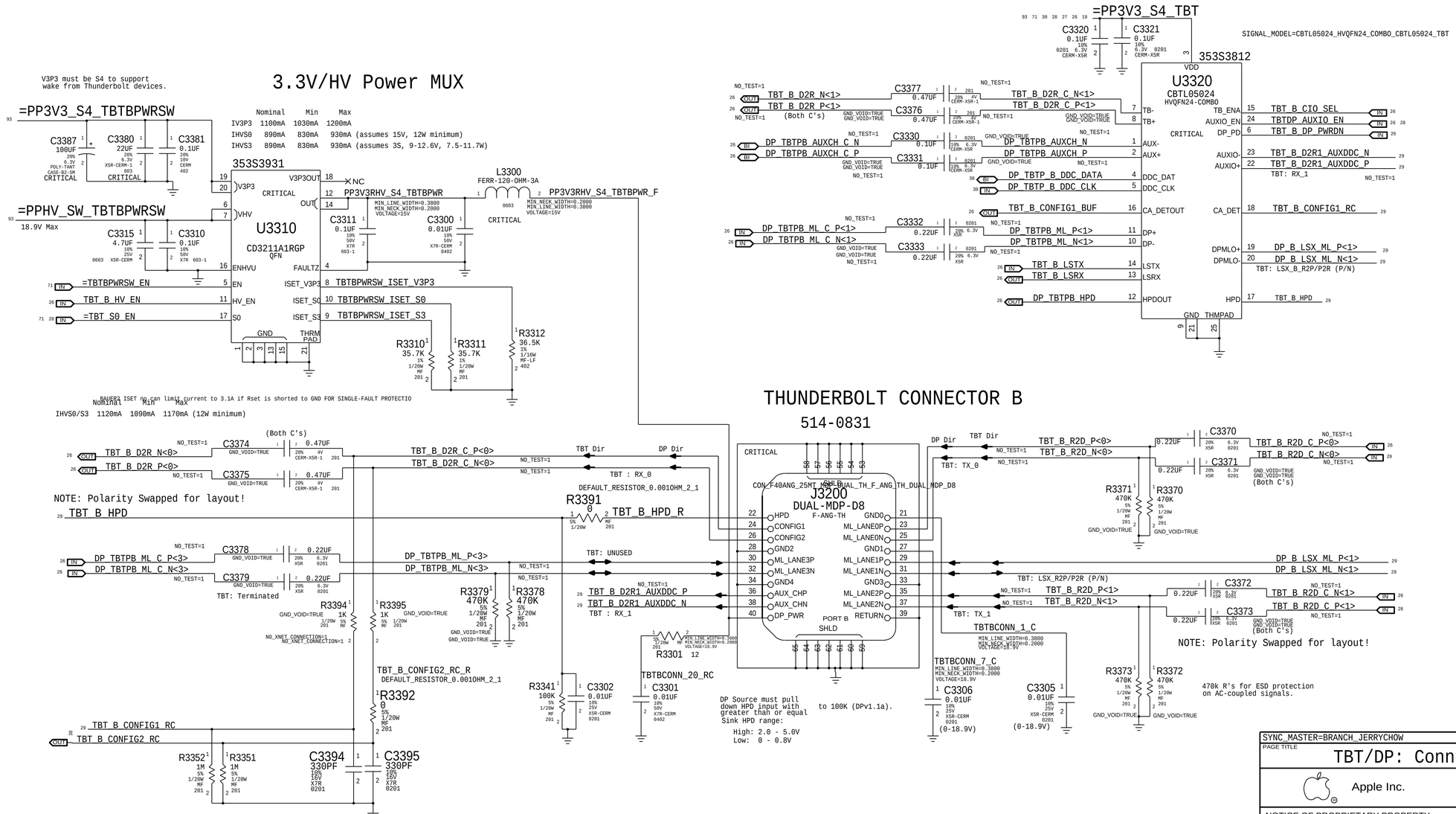

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PAGE TITLE

TBT/DP: Connector B

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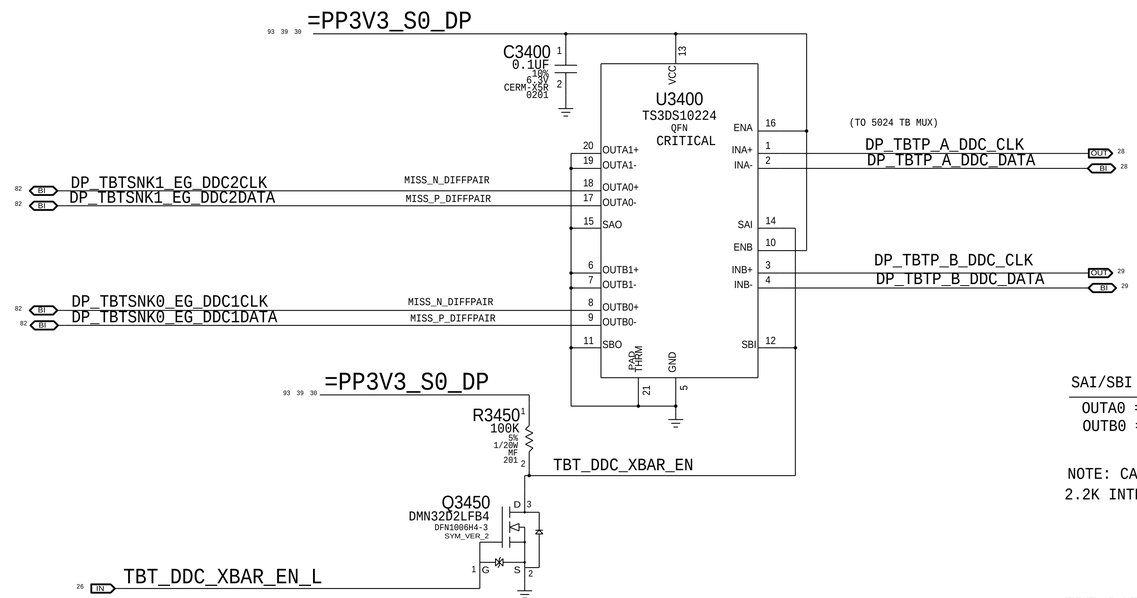
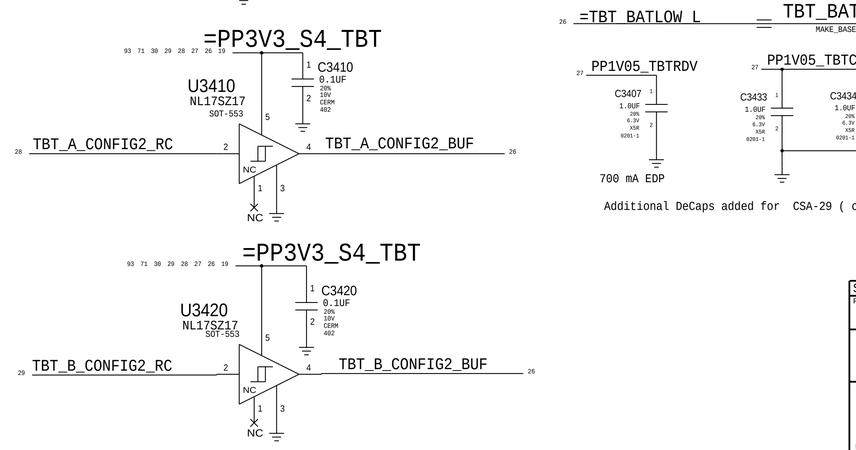
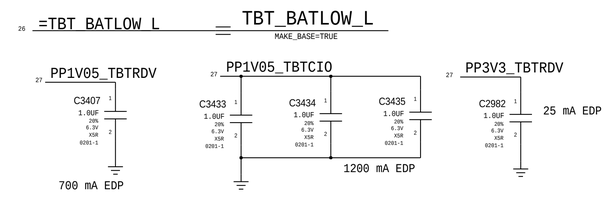
Dual-Port Host DDC Crossbar



SAI/SBI =	0	1
OUTA0 =	INB	INA
OUTB0 =	INA	INB

NOTE: CABLE ADAPTERS ARE REQUIRED TO HAVE 2.2K INTERNAL PULL-UPS.





Additional DeCaps added for CSA-29 (csa-29 is syncing from J44)

SYNC_MASTER=BRANCH_JERRYCHOW SYNC_DATE=11/05/2014

PAGE TITLE
TBT/DP: DDC Crossbar

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D
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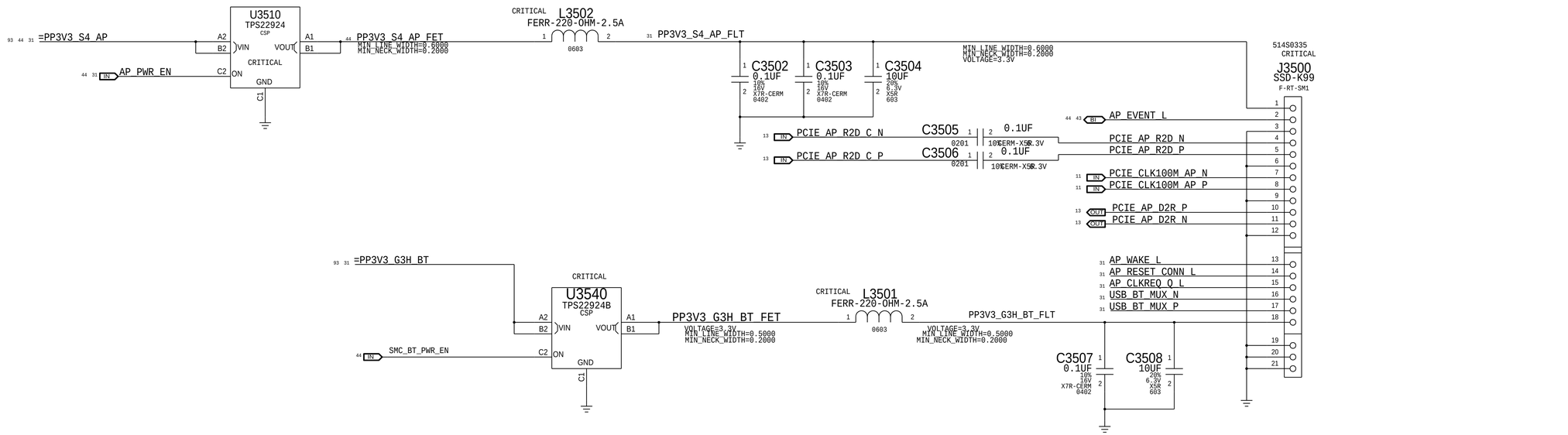
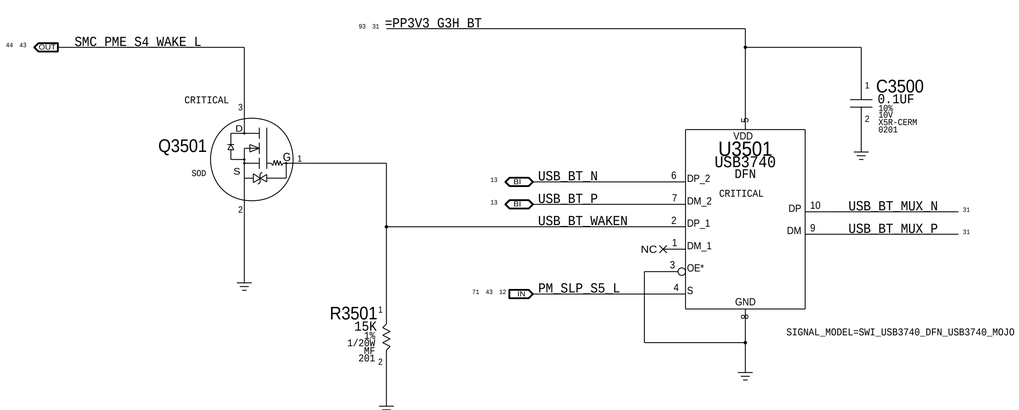
AIRPORT BLUETOOTH

AP & BT Load Switch

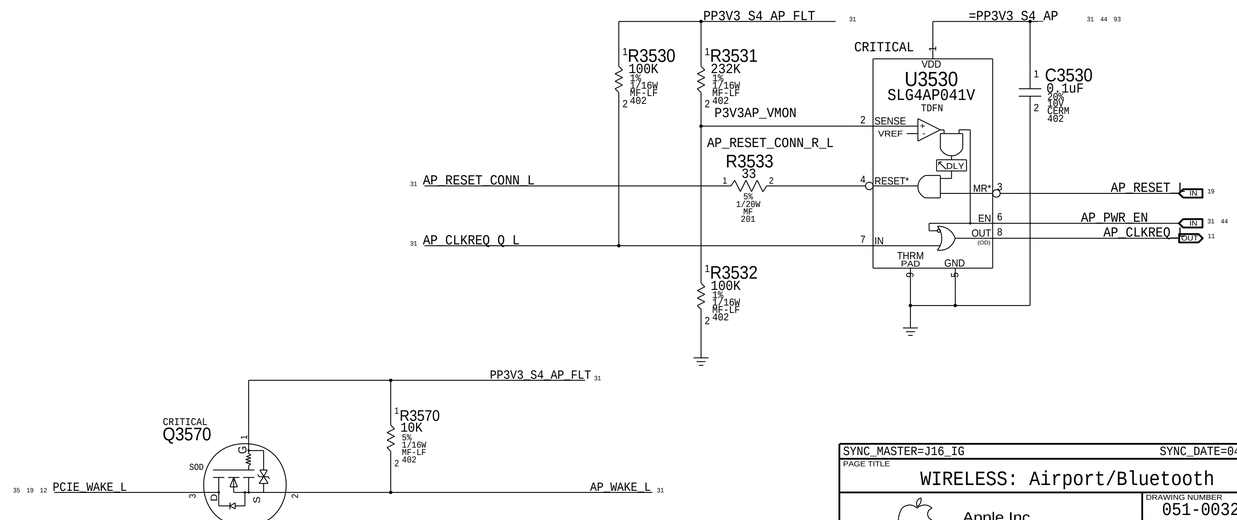
SWITCH	TPS22924B
CHANNEL	N-TYPE
RDS(ON)	18.4 MOHM @3.3V
LOADING	2 A (EDP)



Wake from BT in G3H circuit



Supervisor & CLKREQ# Isolation
Delay = 130 ms +/- 20%



SYNC_MASTER=J16_IG SYNC_DATE=04/29/2013

PAGE TITLE
WIRELESS: Airport/Bluetooth

Apple Inc.

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BRANCH proto1b
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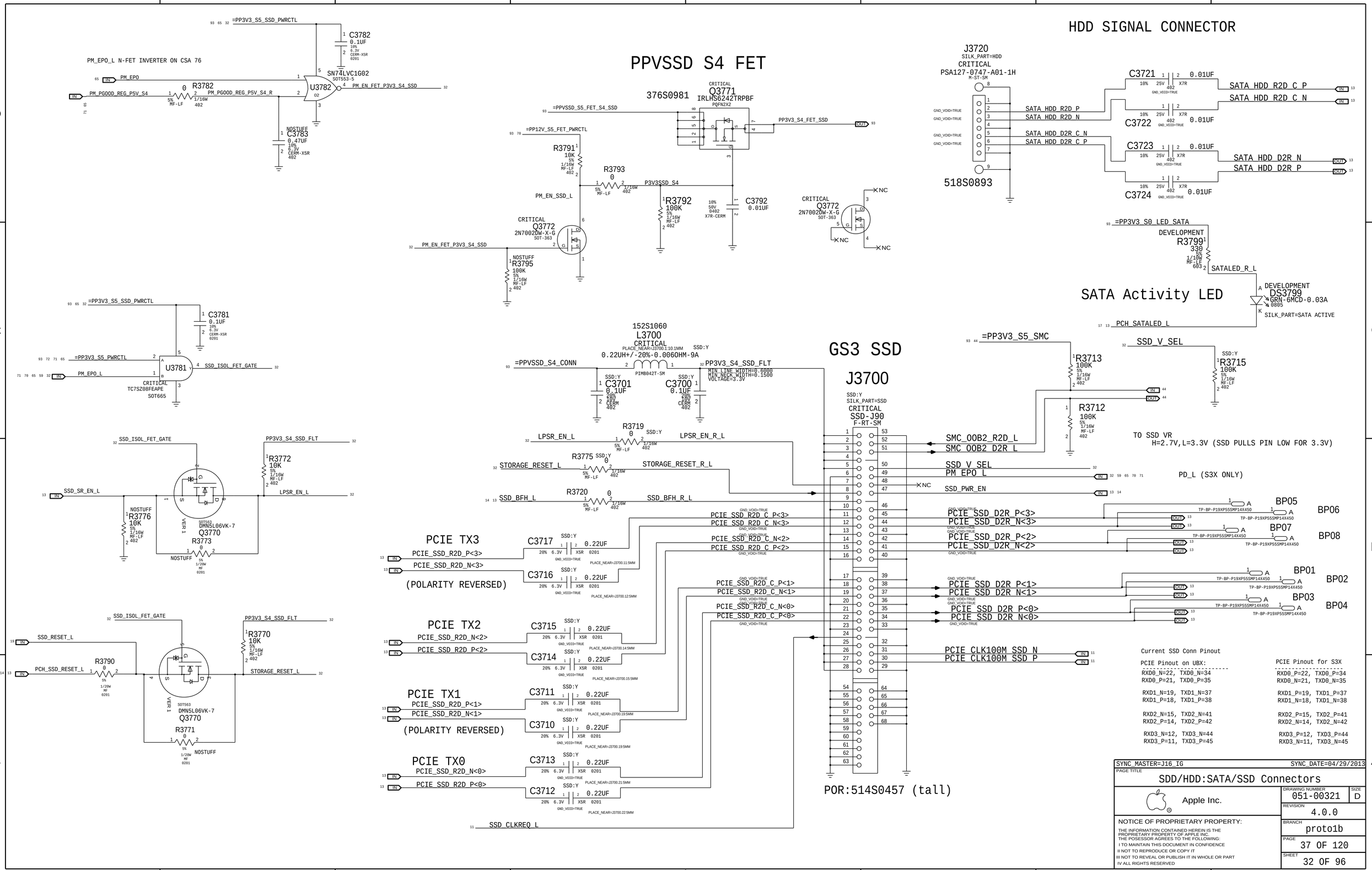
PPVSSD S4 FET
HDD SIGNAL CONNECTOR
SATA Activity LED
GS3 SSD
J3700
SSD-J90
POR:514S0457 (tall)
PCIE TX3
PCIE TX2
PCIE TX1
PCIE TX0
(POLARITY REVERSED)
J3720
518S0893
O3771
IRLHS6242TRPBF
O3772
2N7002DW-X-G
U3782
SN74LVC1G02
U3781
TC7SZ08FEAPE
Q3770
DMN5L06VK-7
DS3799
GRN-6MCD-0.03A
TO SSD VR
H=2.7V,L=3.3V (SSD PULLS PIN LOW FOR 3.3V)
PD_L (S3X ONLY)
Current SSD Conn Pinout
PCIE Pinout on UBX:
RXD0_N=22, TXD0_N=34
RXD0_P=21, TXD0_P=35
RXD1_N=19, TXD1_N=37
RXD1_P=18, TXD1_P=38
RXD2_N=15, TXD2_N=41
RXD2_P=14, TXD2_P=42
RXD3_N=12, TXD3_N=44
RXD3_P=11, TXD3_P=45
PCIE Pinout for S3X
RXD0_P=22, TXD0_P=34
RXD0_N=21, TXD0_N=35
RXD1_P=19, TXD1_P=37
RXD1_N=18, TXD1_N=38
RXD2_P=15, TXD2_P=41
RXD2_N=14, TXD2_N=42
RXD3_P=12, TXD3_P=44
RXD3_N=11, TXD3_N=45
SYNC_MASTER=J16_IG
SYNC_DATE=04/29/2013
PAGE TITLE
SDD/HDD:SATA/SSD Connectors
Apple Inc.
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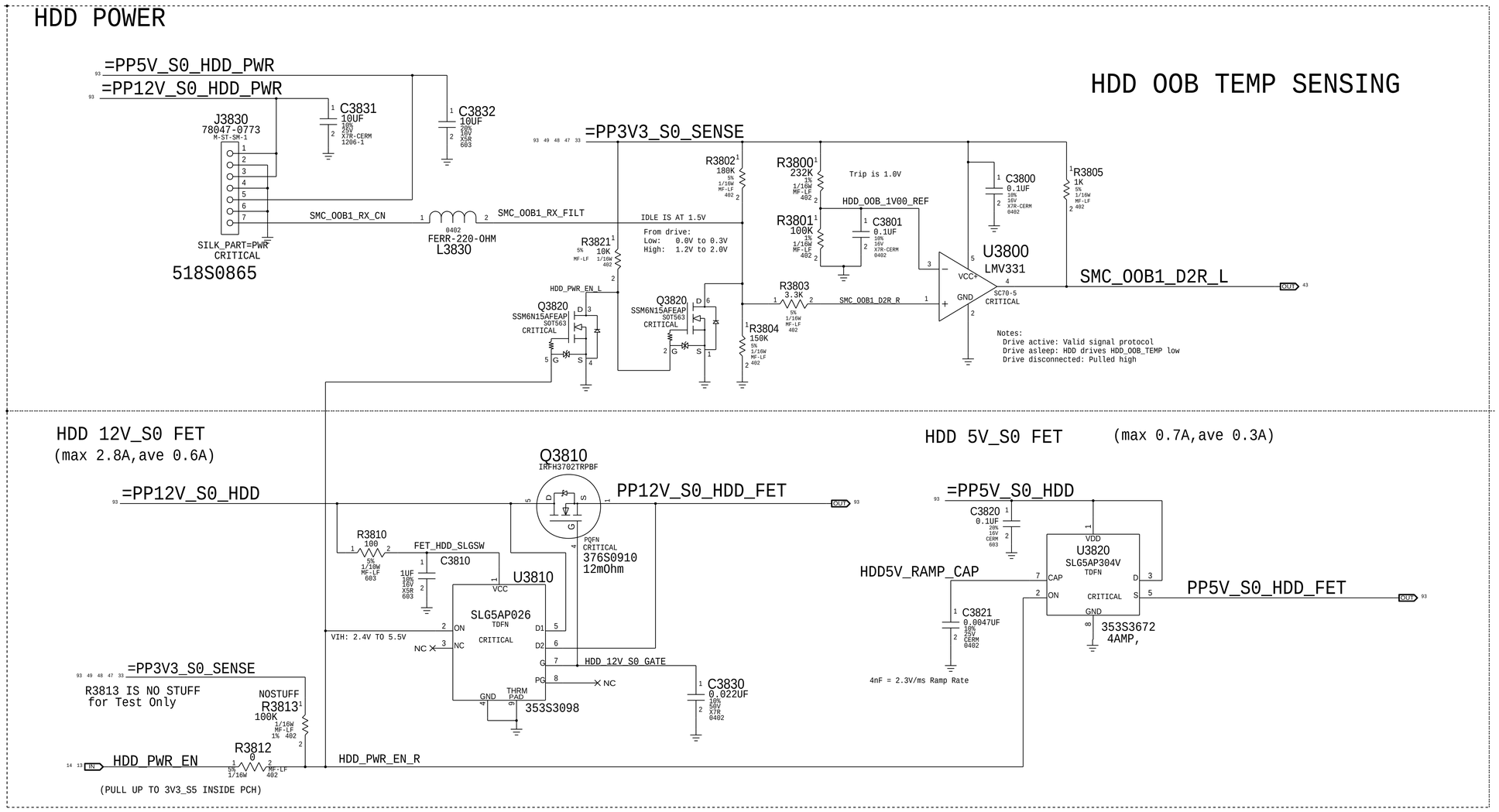

REMOVE R3813 AND SHORT R3812 AFTER HDD_PWR_EN WORKS

SYNC_MASTER=J78_KENNY SYNC_DATE=03/10/2014

PAGE TITLE
HDD: SSD Temp Sense

Apple Inc.

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

=PP3V3_ENET_PHY
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
=PP3V3R1V8_CR_VDDIO

CRITICAL L3900 FERR-600-OHM-300MA-0.85OHM 0402
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C3900 0.1UF 10% 16V X5R-CERM 0201
ENET_XTALVDDH MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V

CRITICAL L3905 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_ENET_PHY_BIASVDDH MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3910 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_ENET_PHY_AVDDH MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
R3910 4.7K 5% 1/10W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201

R3940 4.7K 5% 1/10W MF-LF 402
R3941 4.7K 5% 1/10W MF-LF 402
C3915 4.7UF 20% 6.3V X5R-CERM 402
C3916 0.1UF 10% 16V X5R-CERM 0201

ENET_SR_LX
=ENET_SR_VFB
Internal 1.2V Switching Regulator pins.

=PP1V2_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL L3920 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_ENET_PHY_AVDDL MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500 VOLTAGE=1.2V
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3925 FERR-600-OHM-0.5A SM
PP1V2_ENET_PHY_PCIEPLL MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3930 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_ENET_PHY_GPHYPLL MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500 VOLTAGE=1.2V
C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O. Connect only to U3900 pin 20.

=PP3V3_S0_ENET
R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

C3950 0.1UF 10% 16V X5R-CERM 0201
C3951 0.1UF 10% 16V X5R-CERM 0201
C3955 0.1UF 10% 16V X5R-CERM 0201
C3956 0.1UF 10% 16V X5R-CERM 0201

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
=ENET_WAKE_L (See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

OMIT_TABLE
U3900
BCM57766C0KMLG
QFN-8X8

Pin	Signal	Net	Dir
58	VMAIN_PRSNT (IPD-ENET)	ENET_VMAIN_PRSNT	
27	PCIE_TXD_N	PCIE_ENET_D2R_C_N	
28	PCIE_TXD_P	PCIE_ENET_D2R_C_P	
33	PCIE_RXD_P	PCIE_ENET_R2D_P	
34	PCIE_RXD_N	PCIE_ENET_R2D_N	
31	PCIE_REFCLK_P	PCIE_CLK100M_ENET_P	IN
30	PCIE_REFCLK_N	PCIE_CLK100M_ENET_N	IN
11	PERST* (IPD)	ENET_RESET_L	IN
12	CLKREQ* (OD)	ENET_CLKREQ_L	OUT
3	WAKE* (OD)	=ENET_WAKE_L	OUT
4	LOW_PWR (IPD)	ENET_LOW_PWR	IN
6	SMB_CLK	SMB_ENET_SCL	
10	SMB_DATA (IPD-ENETM)	SMB_ENET_SDA	
66	SCLK_SPD1000LED*	ENET_SCLK	
64	SI/EEDATA	ENET_MISO	
65	SO_LINKLED*	ENET_MOSI	
63	CS*/EECLK	ENET_CS_L	
2	SPD100LED*/SERIAL_DO (OD)	NC	
67	TRAFFICLED*/SERIAL_DI (OD)	ENET_TRAFFICLED_L	OUT
18	XTALI	ENET_XTAL_IN	
19	XTALO	ENET_XTAL_OUT	
38	RDAC	ENET_RDAC	
69	THRM_PAD		

(IPU)

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT can only be used active low due to errata.

Pin	Signal	Net
40	TRD0_P	ENETCONN_MDI_P<0>
41	TRD0_N	ENETCONN_MDI_N<0>
44	TRD1_P	ENETCONN_MDI_P<1>
43	TRD1_N	ENETCONN_MDI_N<1>
46	TRD2_P	ENETCONN_MDI_P<2>
47	TRD2_N	ENETCONN_MDI_N<2>
50	TRD3_P	ENETCONN_MDI_P<3>
49	TRD3_N	ENETCONN_MDI_N<3>
5	GPIO_0/CR_ACT_LED*	NC
8	GPIO_1/LR_OUT	PP3V3R1V8_ENET_LR_OUT
9	GPIO_2/MEDIA_SENSE	ENET_MEDIA_SENSE
1	SD_DETECT* (IPx-ENET)	ENET_SD_DETECT_L
26	CR_CMD (IPU-ENET)	ENET_SD_CMD — R3961 33 5% 1/20W MF 201 — SDCONN_CMD
21	CR_CLK	ENET_SD_CLK — R3979 33 5% 1/20W MF 201 — SDCONN_CLK
25	CR_DATA0	ENET_CR_DATA<0> — R3971 33 5% 1/20W MF 201 — SDCONN_DATA<0>
24	CR_DATA1	ENET_CR_DATA<1> — R3972 33 5% 1/20W MF 201 — SDCONN_DATA<1>
23	CR_DATA2	ENET_CR_DATA<2> — R3973 33 5% 1/20W MF 201 — SDCONN_DATA<2>
22	CR_DATA3	ENET_CR_DATA<3> — R3974 33 5% 1/20W MF 201 — SDCONN_DATA<3>
52	CR_DATA4	NC
53	CR_DATA5	NC
54	CR_DATA6	NC
55	CR_DATA7	NC
59	MS_INS* (IPU-ENET)	NC
60	CR_LED*/CR_BUS_PWR (IPU-ENET)	ENET_CR_PWREN
57	CR_WP* (IPU-ENET)	SDCONN_WP
68	SR_DISABLE (NO IPU OR IPD-ENET)	ENET_SR_DISABLE — R3981 1K 5% 1/16W MF-LF 402

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

(See note)

ENET 1.2V SR IS ENABLED IF FLOATING.

ENET_SR_DISABLE: ENET supports both active-levels for WP.

R3965 1.24K 1% 1/16W MF-LF 402

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

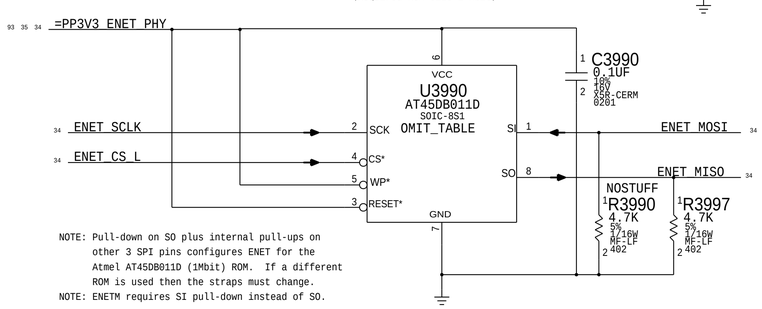
ENET_SR_DISABLE

If ENET switching regulator is used, this pin should have a 1K pull-down to GND

PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900

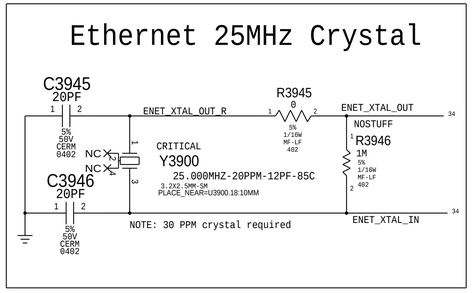
PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)



NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

Ethernet 25MHz Crystal



SYNC_MASTER=J16_IG SYNC_DATE=04/29/2013

PAGE TITLE
ETHERNET: PHY (CAESAR IV)

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D
REVISION 4.0.0
BRANCH proto1b
PAGE 39 OF 120
SHEET 34 OF 96

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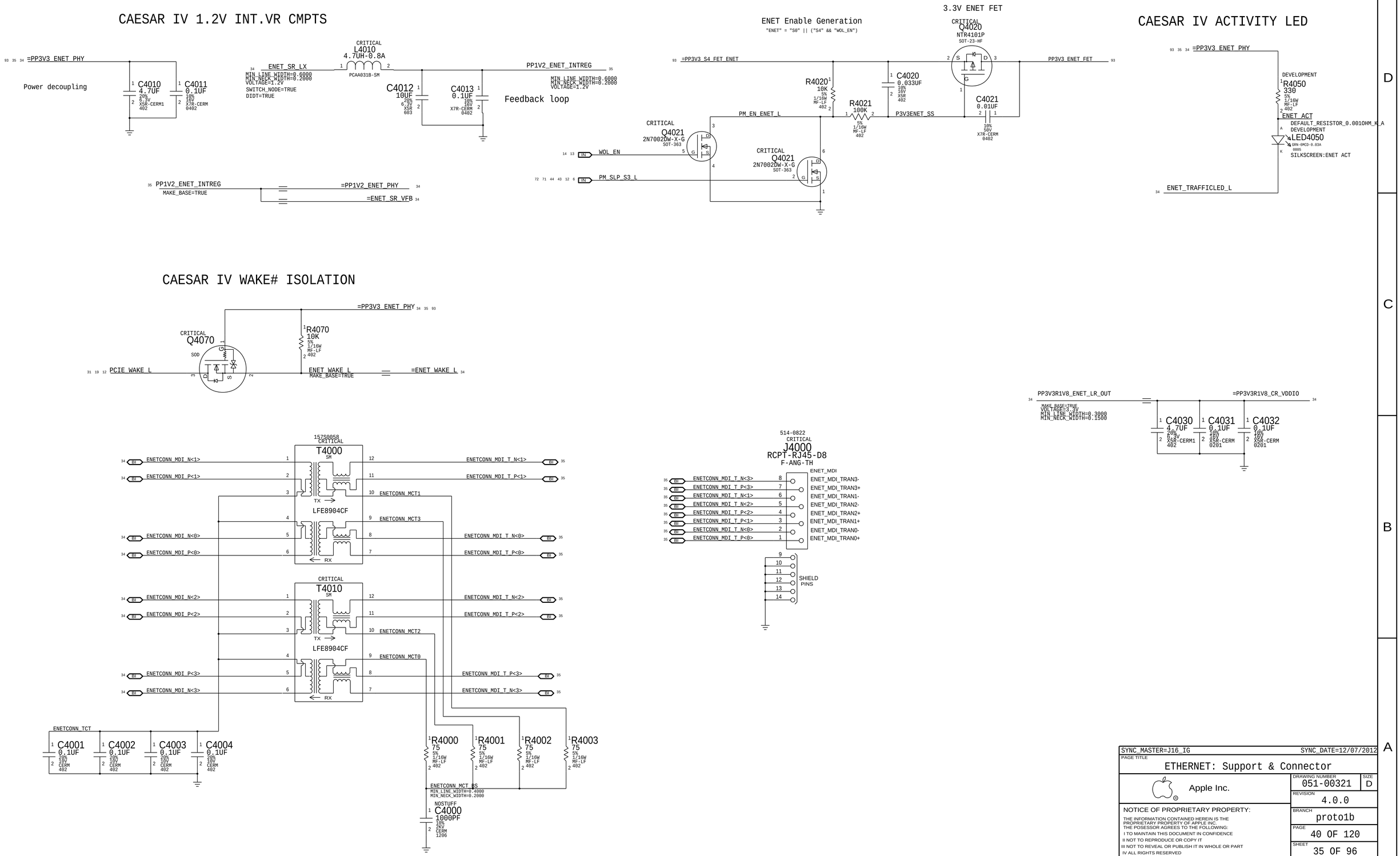
CAESAR IV 1.2V INT.VR CMPTS
=PP3V3_ENET_PHY
Power decoupling
C4010 4.7UF 20% 6.3V X5R-CERM1 402
C4011 0.1UF 10% 16V X7R-CERM 0402
CRITICAL
L4010 4.7UH-0.8A
PCAA031B-SM
ENET_SR_LX
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.2V
SWITCH_NODE=TRUE
DIDT=TRUE
C4012 10UF 20% 6.3V X5R 603
C4013 0.1UF 10% 16V X7R-CERM 0402
PP1V2_ENET_INTREG
Feedback loop
PP1V2_ENET_INTREG
MAKE_BASE=TRUE
=PP1V2_ENET_PHY
=ENET_SR_VFB
ENET Enable Generation
"ENET" = "S0" || ("S4" && "WOL_EN")
=PP3V3_S4_FET_ENET
R4020 10K 5% 1/16W MF-LF 402
PM_EN_ENET_L
CRITICAL
Q4021 2N7002DW-X-G SOT-363
WOL_EN
PM_SLP_S3_L
R4021 100K 5% 1/16W MF-LF 402
C4020 0.033UF 10% 16V X5R 402
P3V3ENET_SS
3.3V ENET FET
CRITICAL
Q4020 NTR4101P SOT-23-HF
C4021 0.01UF 10% 50V X7R-CERM 0402
PP3V3_ENET_FET
CAESAR IV ACTIVITY LED
=PP3V3_ENET_PHY
DEVELOPMENT
R4050 330 5% 1/16W MF-LF 402
ENET_ACT
DEFAULT_RESISTOR_0.001OHM_K_A
DEVELOPMENT
LED4050 GRN-0MCD-0.03A 0805
SILKSCREEN:ENET ACT
ENET_TRAFFICLED_L
CAESAR IV WAKE# ISOLATION
=PP3V3_ENET_PHY
CRITICAL
Q4070 SOD
R4070 10K 5% 1/16W MF-LF 402
PCIE_WAKE_L
ENET_WAKE_L
MAKE_BASE=TRUE
=ENET_WAKE_L
PP3V3R1V8_ENET_LR_OUT
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.1500
=PP3V3R1V8_CR_VDDIO
C4030 4.7UF 20% 6.3V X5R-CERM1 402
C4031 0.1UF 10% 16V X5R-CERM 0201
C4032 0.1UF 10% 16V X5R-CERM 0201
15750058
CRITICAL
T4000 SM
LFE8904CF
TX
RX
ENETCONN_MDI_N<1>
ENETCONN_MDI_P<1>
ENETCONN_MDI_N<0>
ENETCONN_MDI_P<0>
ENETCONN_MCT1
ENETCONN_MCT3
CRITICAL
T4010 SM
LFE8904CF
ENETCONN_MDI_N<2>
ENETCONN_MDI_P<2>
ENETCONN_MDI_P<3>
ENETCONN_MDI_N<3>
ENETCONN_MCT2
ENETCONN_MCT0
ENETCONN_TCT
C4001 0.1UF 20% 10V CERM 402
C4002 0.1UF 20% 10V CERM 402
C4003 0.1UF 20% 10V CERM 402
C4004 0.1UF 20% 10V CERM 402
R4000 75 5% 1/16W MF-LF 402
R4001 75 5% 1/16W MF-LF 402
R4002 75 5% 1/16W MF-LF 402
R4003 75 5% 1/16W MF-LF 402
ENETCONN_MCT_BS
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.2000
NOSTUFF
C4000 1000PF 10% 25V CERM 1206
514-0822
CRITICAL
J4000 RCPT-RJ45-D8 F-ANG-TH
ENET_MDI
ENET_MDI_TRAN3-
ENET_MDI_TRAN3+
ENET_MDI_TRAN1-
ENET_MDI_TRAN2-
ENET_MDI_TRAN2+
ENET_MDI_TRAN1+
ENET_MDI_TRAN0-
ENET_MDI_TRAN0+
SHIELD PINS
SYNC_MASTER=J16_IG
SYNC_DATE=12/07/2012
PAGE TITLE
ETHERNET: Support & Connector
Apple Inc.
DRAWING NUMBER
051-00321
SIZE
D
REVISION
4.0.0
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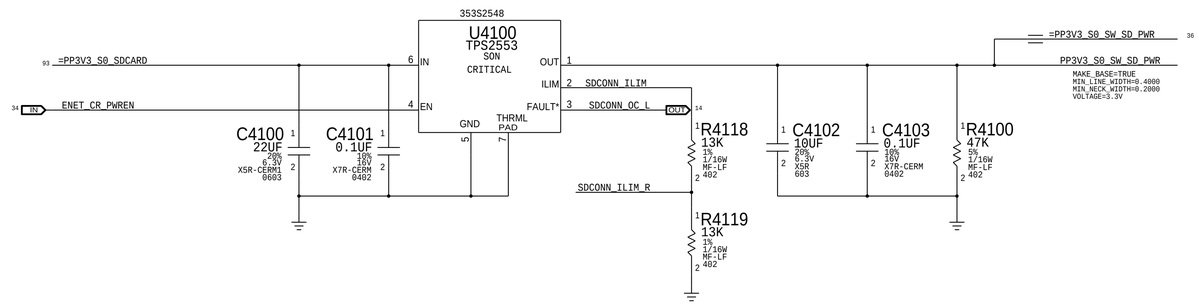
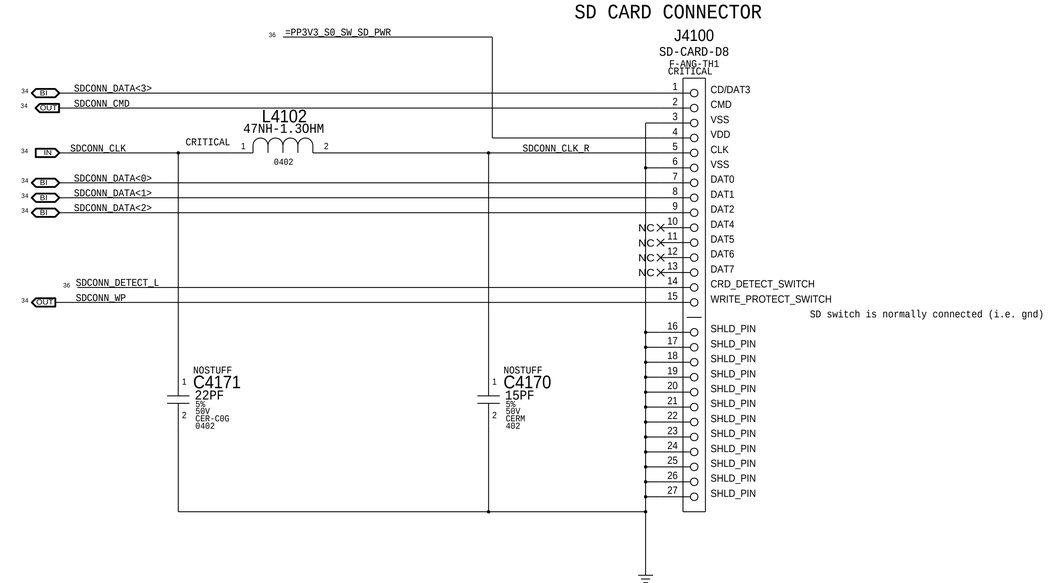
BRANCH
proto1b
PAGE
40 OF 120
SHEET
35 OF 96

SD CARD 3.3V OVERCURRENT PROTECTION CHIP

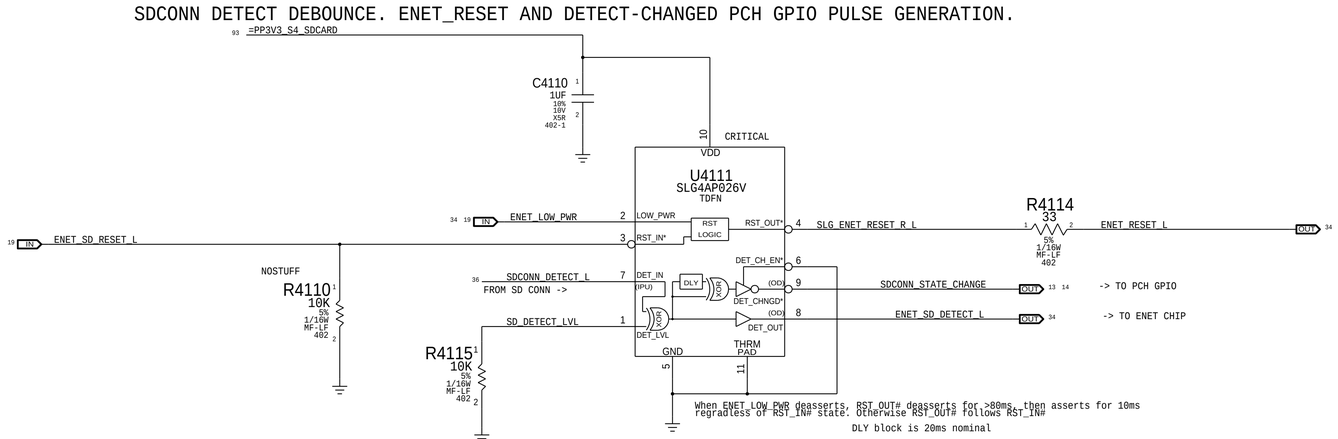


J16:516-0249 / J17:512-0038

SD CARD CONNECTOR



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SYNC_MASTER=J16_IG	SYNC_DATE=04/29/2013
PAGE TITLE: SD CARD: Connector	
Apple Inc.	DRAWING NUMBER: 051-00321 / SIZE: D
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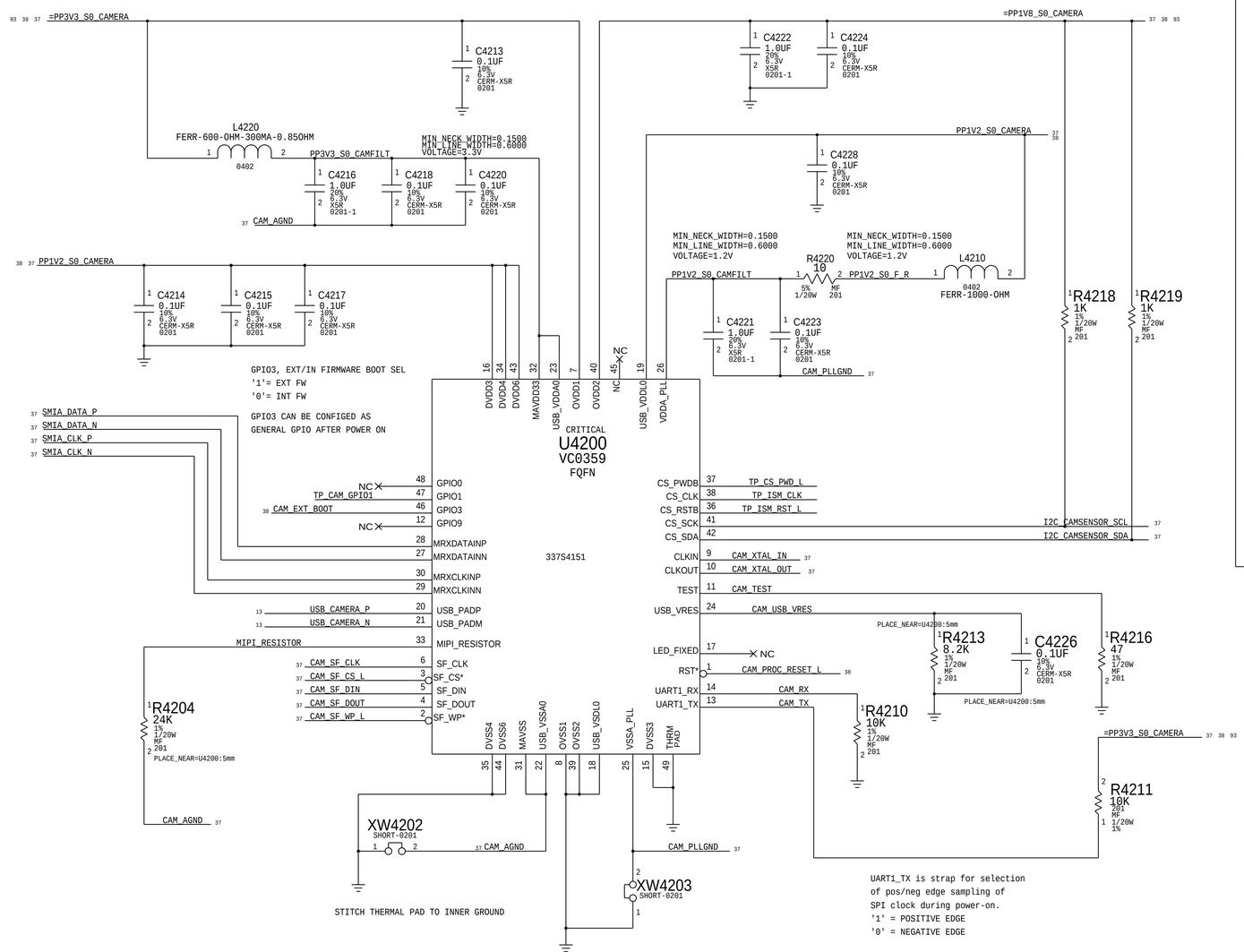
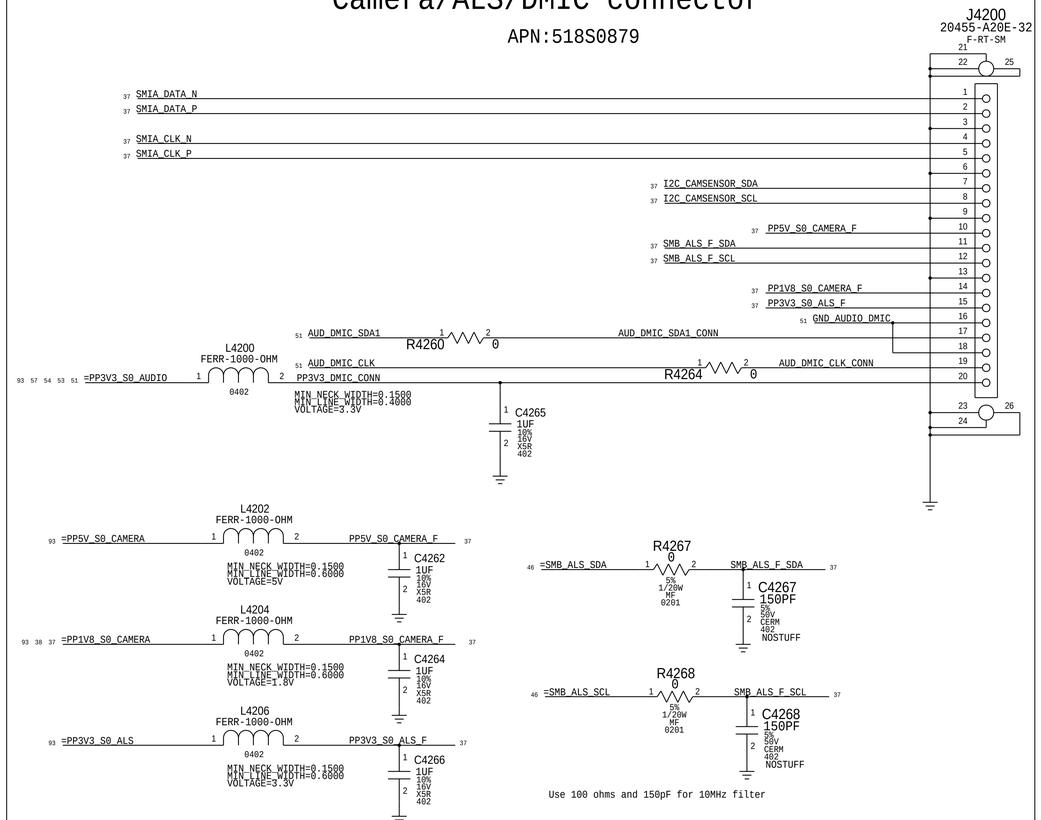
	PAGE: 41 OF 120
	SHEET: 36 OF 96

USB CAMERA CONTROLLER

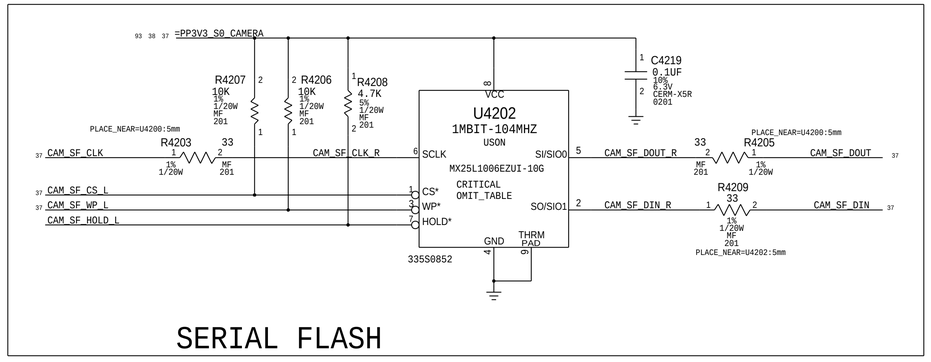


Camera/ALS/DMIC connector

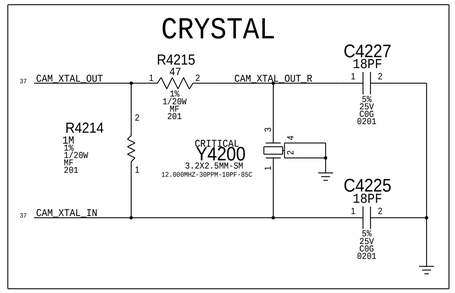
APN:518S0879



SERIAL FLASH



CRYSTAL



SYNC_MASTER=J78_NAT SYNC_DATE=11/05/2013

PAGE TITLE: CAMERA: Controller

Apple Inc.

DRAWING NUMBER: 051-00321 SIZE: D

REVISION: 4.0.0

BRANCH: proto1b

PAGE: 42 OF 120

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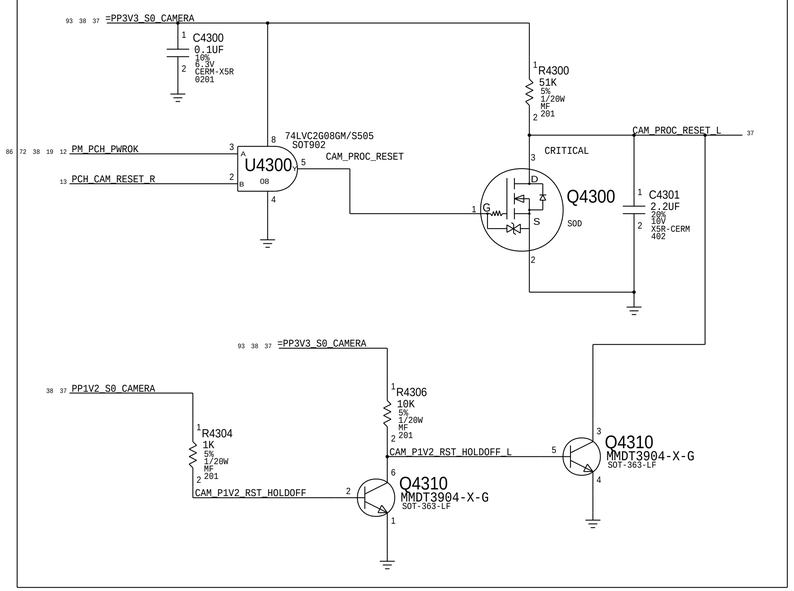
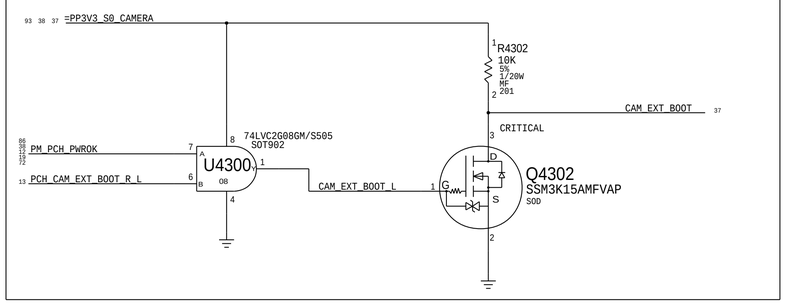
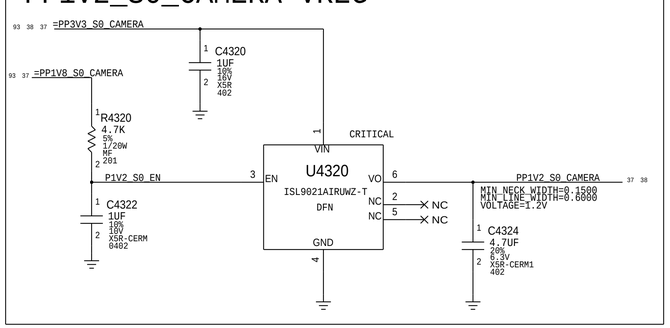
Camera Processor Reset



Camera Processor ExtBoot Cntl



PP1V2_S0_CAMERA VREG



SYNC_MASTER=J78_NAT SYNC_DATE=11/05/2013

PAGE TITLE
CAMERA: Controller Support

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

PAGE 43 OF 120

SHEET 38 OF 96

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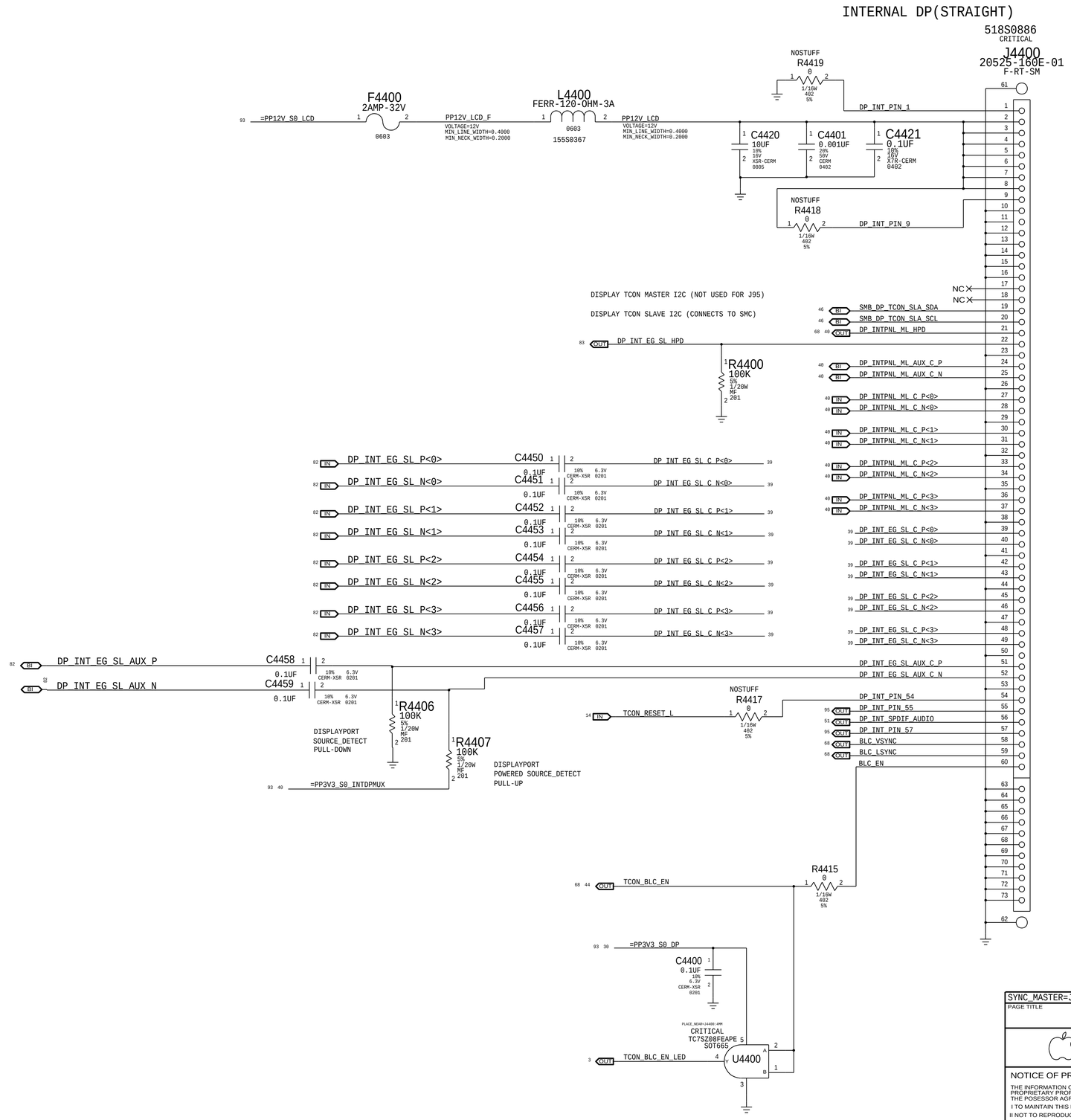

SYNC_MASTER=J95_ANDREW SYNC_DATE=1/27/2015

PAGE TITLE

DISPLAY: Support

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

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PAGE 44 OF 120

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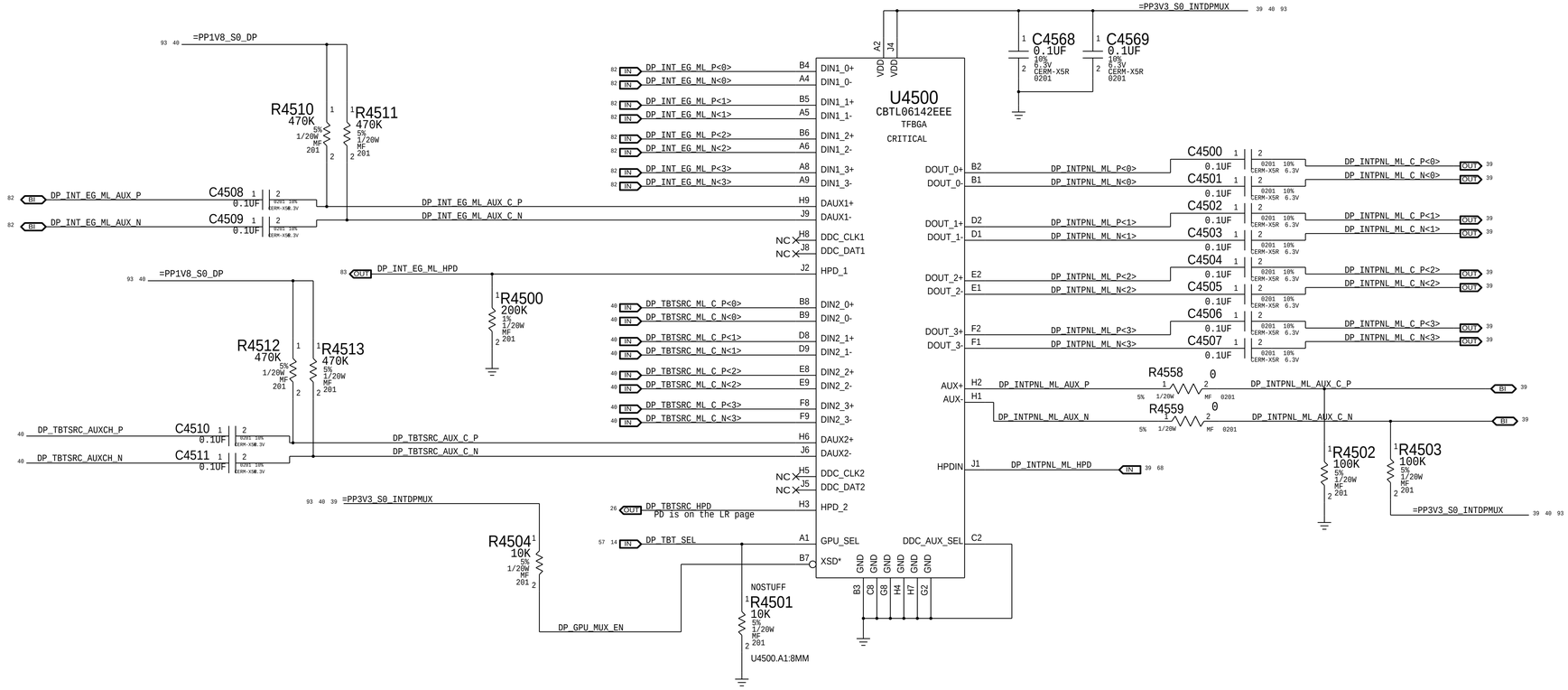
TP to DP aliases

26 IN	TP_DP_TBTSRC_ML_CP<0>	DP_TBTSRC_ML_P<0>	40 (MAKE_BASE=TRUE)
26 IN	TP_DP_TBTSRC_ML_CN<0>	DP_TBTSRC_ML_N<0>	40 (MAKE_BASE=TRUE)
26 IN	TP_DP_TBTSRC_ML_CP<1>	DP_TBTSRC_ML_P<1>	40 (MAKE_BASE=TRUE)
26 IN	TP_DP_TBTSRC_ML_CN<1>	DP_TBTSRC_ML_N<1>	40 (MAKE_BASE=TRUE)
26 IN	TP_DP_TBTSRC_ML_CP<2>	DP_TBTSRC_ML_P<2>	40 (MAKE_BASE=TRUE)
26 IN	TP_DP_TBTSRC_ML_CN<2>	DP_TBTSRC_ML_N<2>	40 (MAKE_BASE=TRUE)
26 IN	TP_DP_TBTSRC_ML_CP<3>	DP_TBTSRC_ML_P<3>	40 (MAKE_BASE=TRUE)
26 IN	TP_DP_TBTSRC_ML_CN<3>	DP_TBTSRC_ML_N<3>	40 (MAKE_BASE=TRUE)
26 BI	TP_DP_TBTSRC_AUXCH_CP	DP_TBTSRC_AUXCH_P	40 (MAKE_BASE=TRUE)
26 BI	TP_DP_TBTSRC_AUXCH_CN	DP_TBTSRC_AUXCH_N	40 (MAKE_BASE=TRUE)



40 IN	DP_TBTSRC_ML_P<0>	DP_TBTSRC_ML_C_P<0>	40 (MAKE_BASE=TRUE)
40 IN	DP_TBTSRC_ML_N<0>	DP_TBTSRC_ML_C_N<0>	40 (MAKE_BASE=TRUE)
40 IN	DP_TBTSRC_ML_P<1>	DP_TBTSRC_ML_C_P<1>	40 (MAKE_BASE=TRUE)
40 IN	DP_TBTSRC_ML_N<1>	DP_TBTSRC_ML_C_N<1>	40 (MAKE_BASE=TRUE)
40 IN	DP_TBTSRC_ML_P<2>	DP_TBTSRC_ML_C_P<2>	40 (MAKE_BASE=TRUE)
40 IN	DP_TBTSRC_ML_N<2>	DP_TBTSRC_ML_C_N<2>	40 (MAKE_BASE=TRUE)
40 IN	DP_TBTSRC_ML_P<3>	DP_TBTSRC_ML_C_P<3>	40 (MAKE_BASE=TRUE)
40 IN	DP_TBTSRC_ML_N<3>	DP_TBTSRC_ML_C_N<3>	40 (MAKE_BASE=TRUE)

SYNC_MASTER=J78_KENNY SYNC_DATE=10/09/2013

PAGE TITLE
DISPLAY: MUXing

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D
REVISION 4.0.0
BRANCH proto1b
PAGE 45 OF 120
SHEET 40 OF 96

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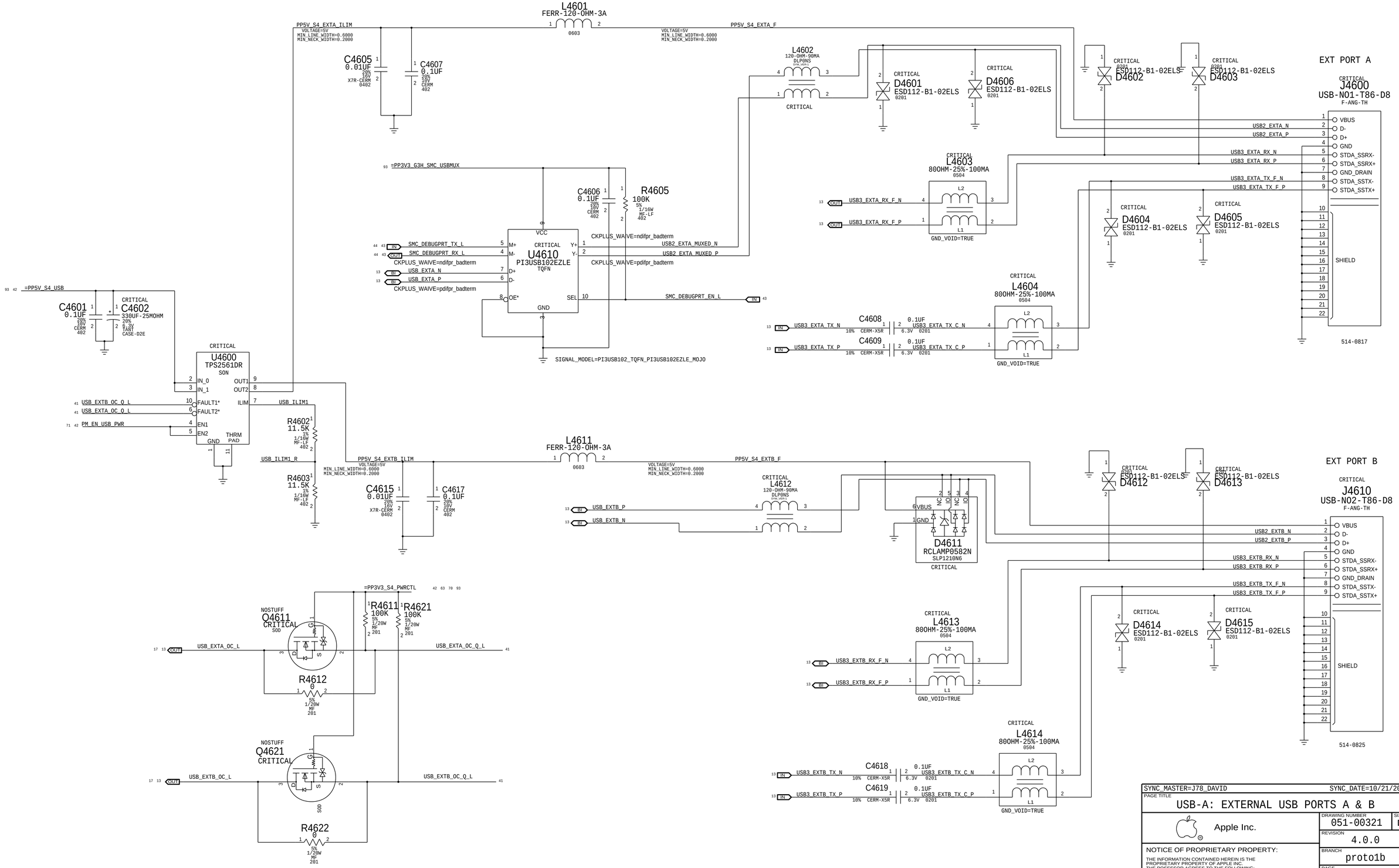

SYNC_MASTER=J78_DAVID SYNC_DATE=10/21/2013

PAGE TITLE

USB-A: EXTERNAL USB PORTS A & B

Apple Inc.

DRAWING NUMBER	051-00321
SIZE	D
REVISION	4.0.0
BRANCH	proto1b
PAGE	46 OF 120
SHEET	41 OF 96

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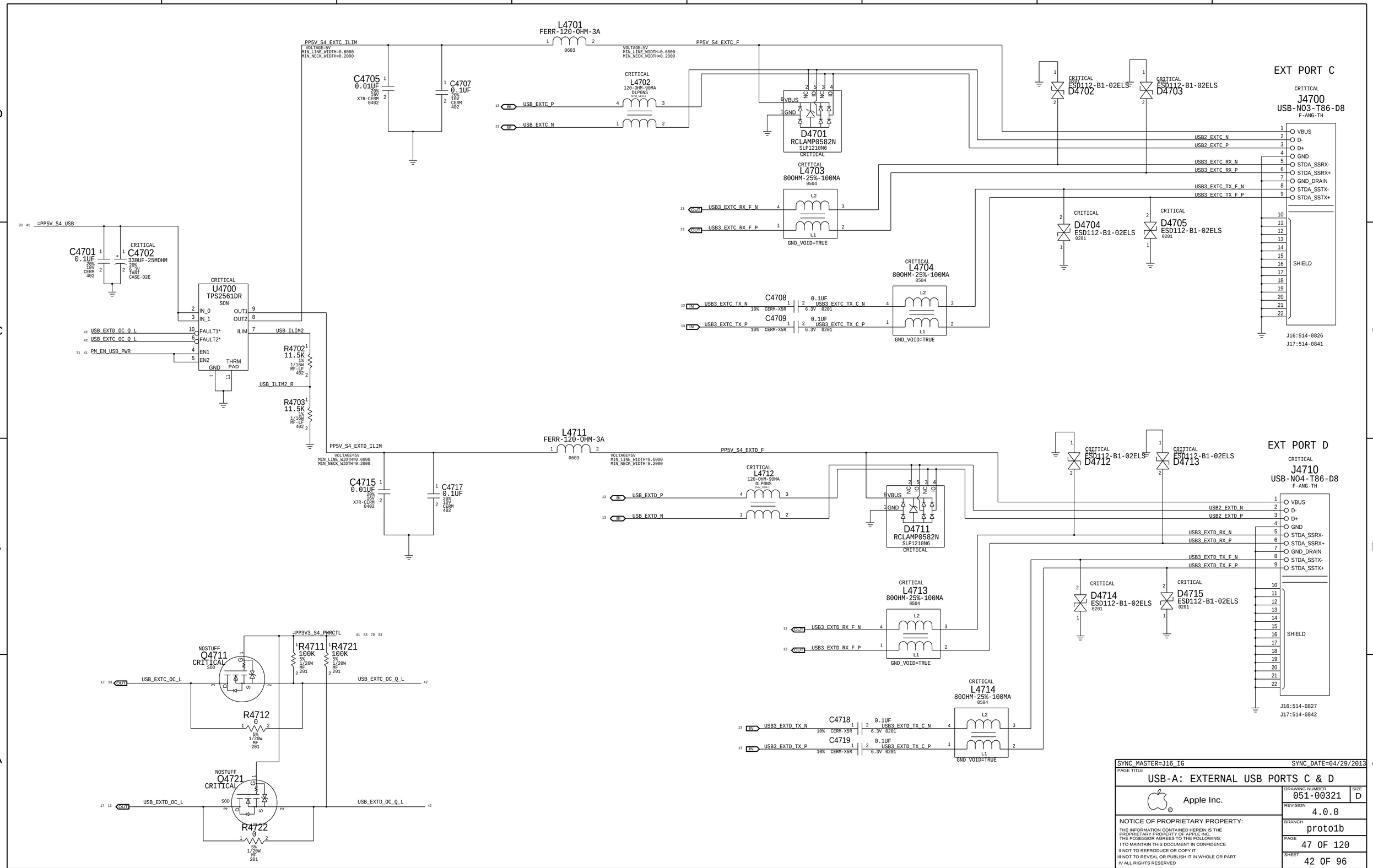

SYNC_MASTER=J16_IG SYNC_DATE=04/29/2013

PAGE TITLE
USB-A: EXTERNAL USB PORTS C & D

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D
REVISION 4.0.0
BRANCH proto1b
PAGE 47 OF 120
SHEET 42 OF 96

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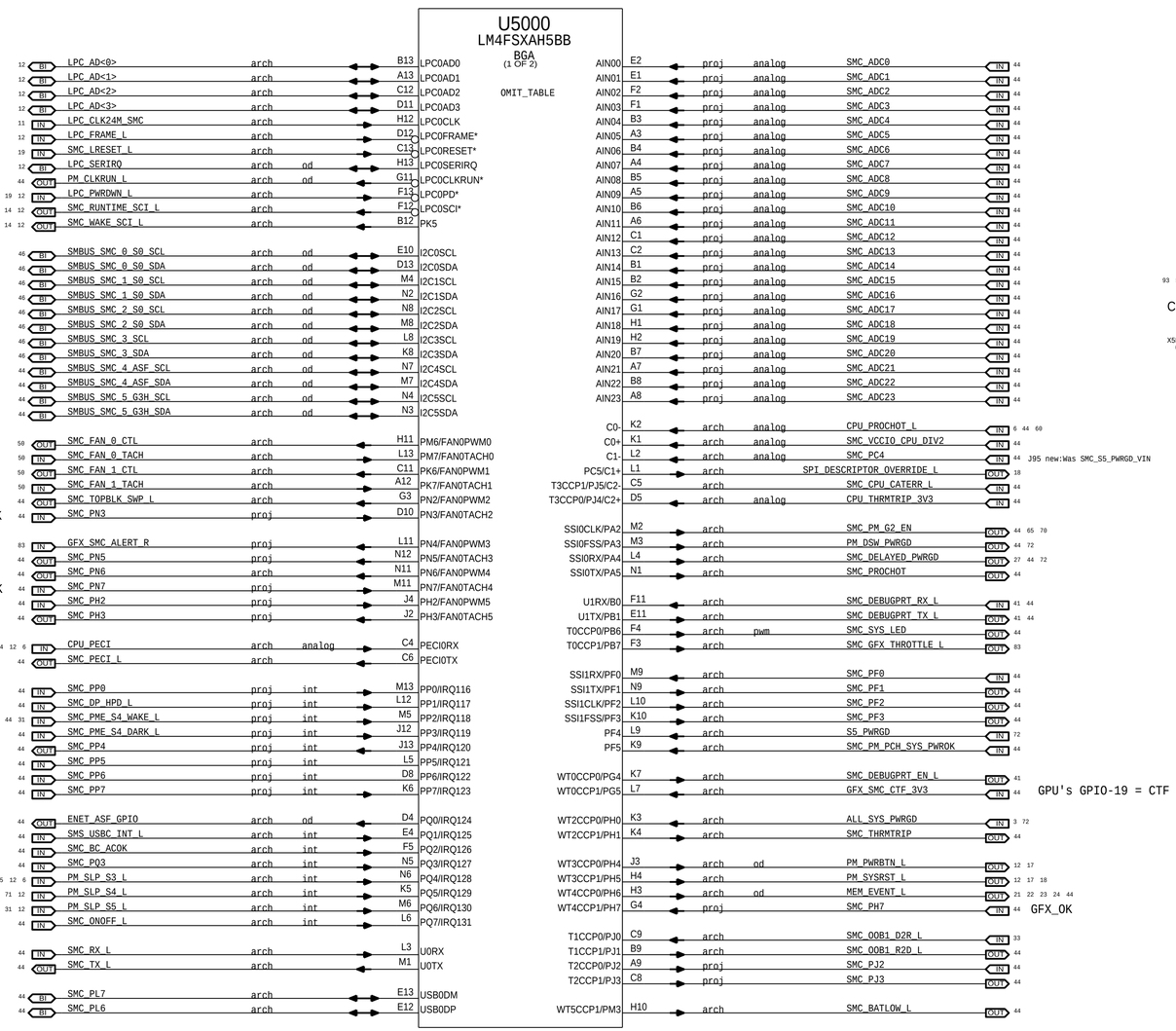
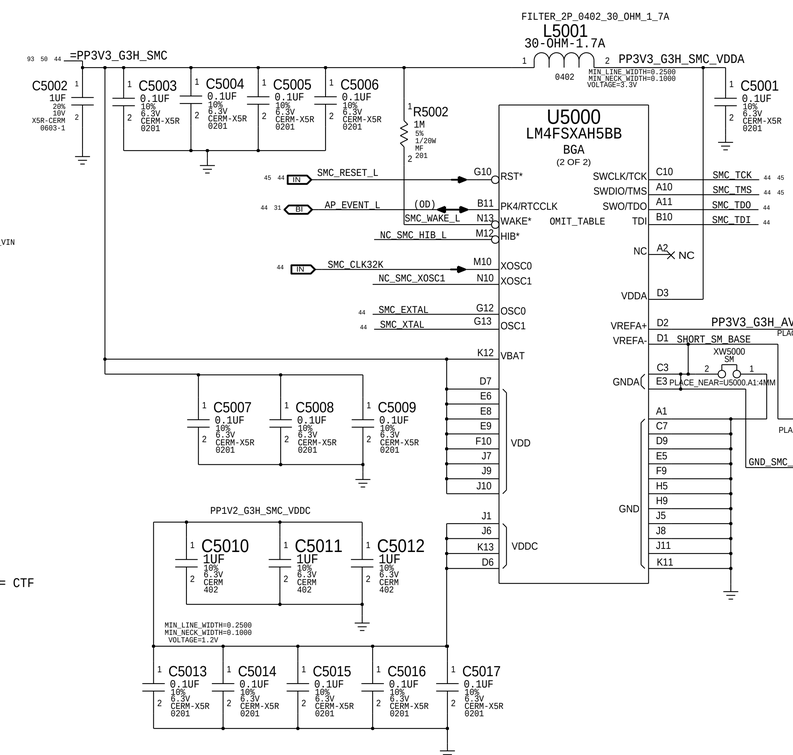
NOTE: Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.





SYNC_MASTER=BRANCH_JERRYCHOW SYNC_DATE=11/06/2014

PAGE TITLE

SMC: Controller

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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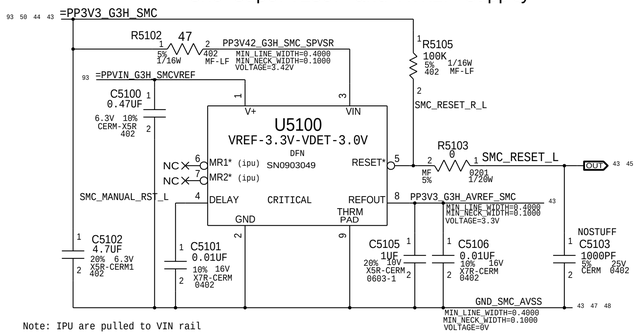
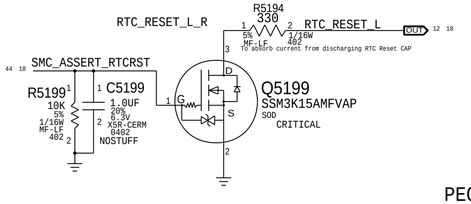
SMC Supervisor and AVREF Supply

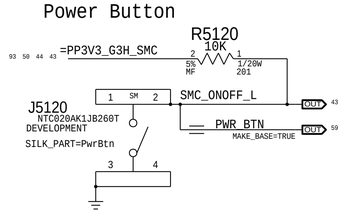


Note: IPU are pulled to VIN rail

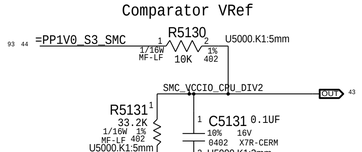
SMC Controlled RTC Reset



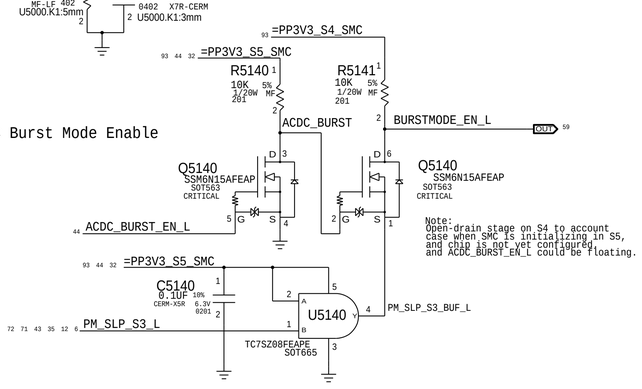
Power Button



Comparator VRef

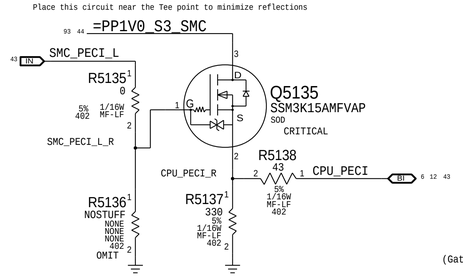


AC/DC Burst Mode Enable



PECI Support

Level-shifter that allows SMC to drive PECI
Place this circuit near the Tee point to minimize reflections



ADC Channel Aliases

SMC_ADC0	VSNS_P12VG3H	MAKE_BASE=TRUE	VD2R
SMC_ADC1	ISNS_P12VG3H	MAKE_BASE=TRUE	ID2R
SMC_ADC2	VSNS_P12VS0_CPUCORE	MAKE_BASE=TRUE	VD20
SMC_ADC3	ISNS_P12VS0_CPUCORE	MAKE_BASE=TRUE	ID20
SMC_ADC4	VSNS_CPUVCC	MAKE_BASE=TRUE	VC0C
SMC_ADC5	ISNS_CPUVCC	MAKE_BASE=TRUE	IC0C
SMC_ADC6	VSNS_CPUVCC_GT	MAKE_BASE=TRUE	VC0G
SMC_ADC7	ISNS_CPUVCC_GT	MAKE_BASE=TRUE	IC0G
SMC_ADC8	ISNS_CPUVCC_IO	MAKE_BASE=TRUE	IC0I
SMC_ADC9	ISNS_P1V35S0	MAKE_BASE=TRUE	IC0M
SMC_ADC10	ISNS_CPUVCC_SA	MAKE_BASE=TRUE	IC0S
SMC_ADC11	ISNS_P12VS0_FBVDDQ	MAKE_BASE=TRUE	IG1F
SMC_ADC12	VSNS_GPUCORE_ALT	MAKE_BASE=TRUE	VG0C
SMC_ADC13	ISNS_GPUCORE_ALT	MAKE_BASE=TRUE	IG0C
SMC_ADC14	VSNS_GPU_VDDCI	MAKE_BASE=TRUE	VG0I
SMC_ADC15	ISNS_GPU_VDDCI	MAKE_BASE=TRUE	IG0I
SMC_ADC16	ISNS_P12VS0_GPU_AUX	MAKE_BASE=TRUE	IG1A
SMC_ADC17	ISNS_P12VS0_GPUCORE	MAKE_BASE=TRUE	IG1C
SMC_ADC18	ISNS_P12VS0_HDD	MAKE_BASE=TRUE	IH02
SMC_ADC19	ISNS_HDDS0	MAKE_BASE=TRUE	IH05
SMC_ADC20	VSNS_SSD_S4	MAKE_BASE=TRUE	VH1R
SMC_ADC21	ISNS_SSD_S4	MAKE_BASE=TRUE	IH1R
SMC_ADC22	VSNS_VDDQS3_DDR	MAKE_BASE=TRUE	VM0R
SMC_ADC23	ISNS_VDDQS3_DDR	MAKE_BASE=TRUE	IM0R

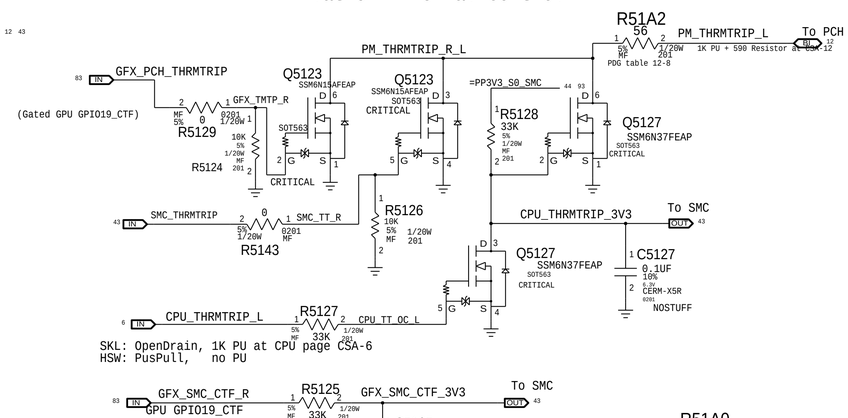
Project-specific Aliases

SMC_PN5	ACDC_BURST_EN_L	MAKE_BASE=TRUE	
SMC_PJ3	SMC_OOB2_R2D_L	MAKE_BASE=TRUE	
SMC_PJ2	SMC_OOB2_D2R_L	MAKE_BASE=TRUE	
SMC_PP0	SMC_ACDC_ID	MAKE_BASE=TRUE	
SMC_PH2	SMC_ASSERT_RTCRST	MAKE_BASE=TRUE	
SMC_PL6	SMC_WIFI_PWR_EN	MAKE_BASE=TRUE	
SMC_PN3	TCON_BLC_EN	MAKE_BASE=TRUE	(LED-4) (100K PD AT BLC)
SMC_PH7	GFX_OK_L	MAKE_BASE=TRUE	(LED-3) (5K PU AT MLB)
SMC_PN7	DP_LINK_OK	MAKE_BASE=TRUE	(LED-3)

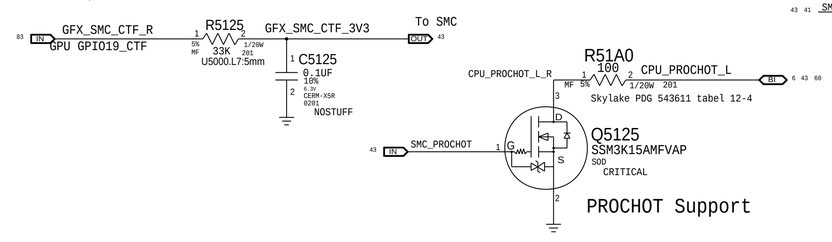
Unused Project-specific

SMC_PF0	NC_SMC_PF0	MAKE_BASE=TRUE	
SMC_PF1	NC_SMC_PF1	MAKE_BASE=TRUE	
SMC_PF2	NC_SMC_PF2	MAKE_BASE=TRUE	
SMC_PF3	NC_SMC_PF3	MAKE_BASE=TRUE	
SMC_PL7	SMC_BT_PWR_EN	MAKE_BASE=TRUE	(J95 new)
SMC_PP4	NC_SMC_S4_WAKESRC_EN	MAKE_BASE=TRUE	
SMC_PP5	NC_SMC_PP5	MAKE_BASE=TRUE NO_TEST=1	
SMC_PP6	NC_SMC_PP6	MAKE_BASE=TRUE NO_TEST=1	
SMC_PP7	NC_SMC_PP7	MAKE_BASE=TRUE NO_TEST=1	
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE NO_TEST=1	
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	MAKE_BASE=TRUE NO_TEST=1	
SMC_PC4	NC_SMC_S5_PWRGD_VIN	MAKE_BASE=TRUE NO_TEST=1	
SMC_PQ3	NC_G3_POWERON_L	MAKE_BASE=TRUE	
SMC_PN6	NC_SMC_G3_WAKESRC_EN	MAKE_BASE=TRUE	
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE	
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE NO_TEST=1	
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	MAKE_BASE=TRUE NO_TEST=1	
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	MAKE_BASE=TRUE NO_TEST=1	
SMC_OOB1_R2D_L	NC_SMC_OOB1_R2D_L	MAKE_BASE=TRUE NO_TEST=1	
SMC_BATLOW_L	NC_SMC_SMC_BATLOW_L	MAKE_BASE=TRUE NO_TEST=1	
SMC_PH3	NC_SMC_PH3	MAKE_BASE=TRUE NO_TEST=1	

Platform Thermal Control

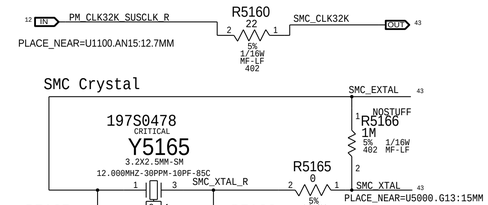


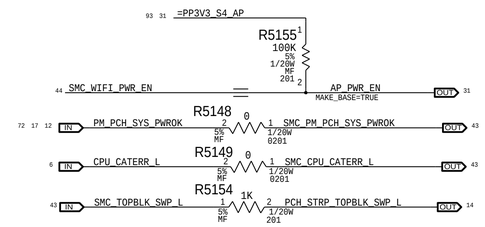
SKL: OpenDrain, 1K PU at CPU page CSA-6
HSW: PusPull, no PU



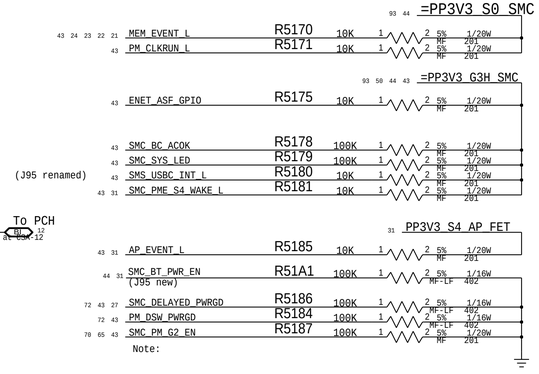
PROCHOT Support

SMC 32KHz Clock

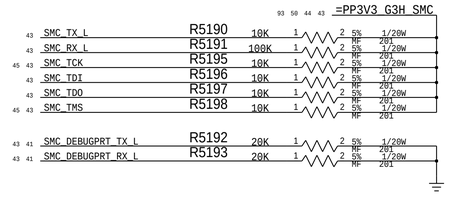




Arch Pull Up/Down



Serial/JTAG Interface Pull-ups



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PAGE TITLE
SMC: Controller Support

Apple Inc.

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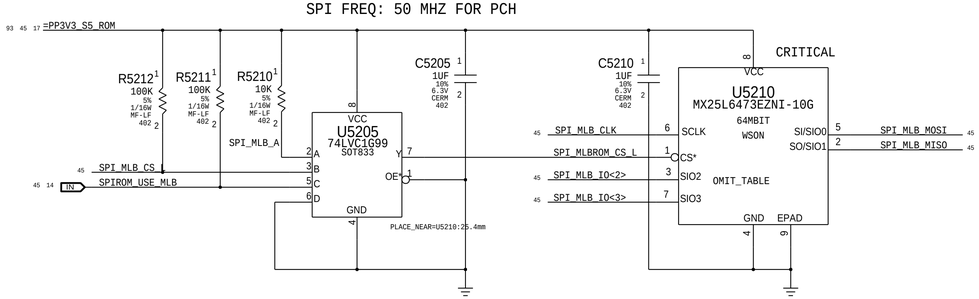
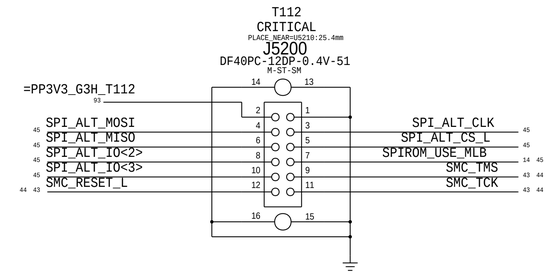
SPI BootROM

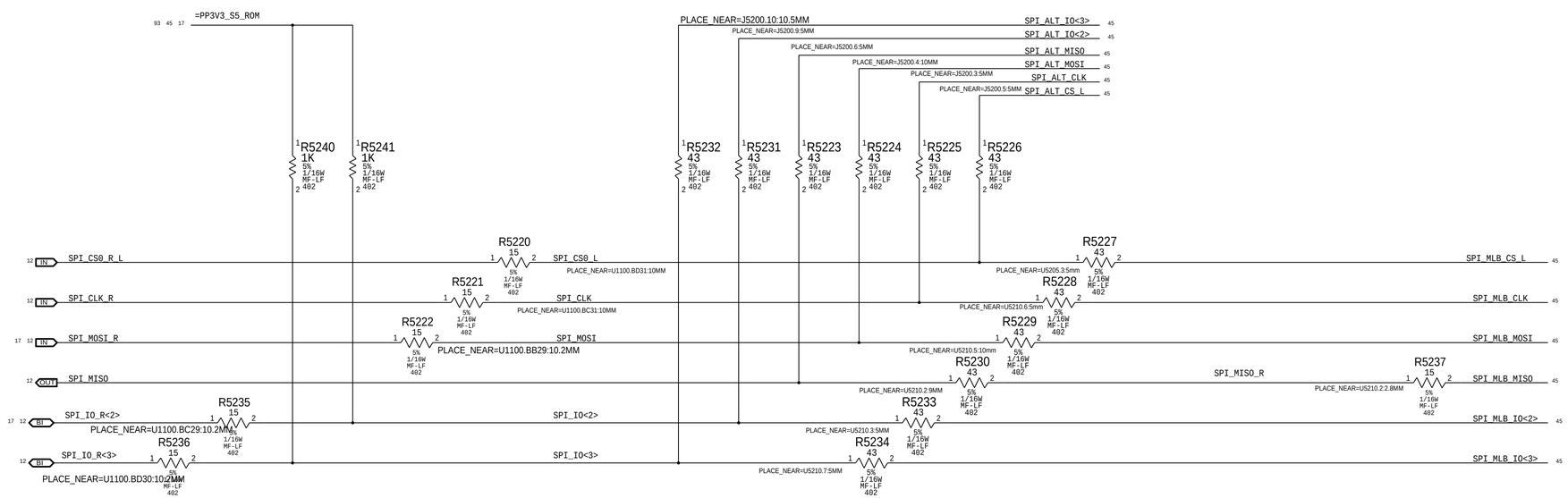
QUAD_IO MODE (MODE 0 & 3) SUPPORTED
SPI FREQ: 50 MHZ FOR PCH



T112 Connector



SPI Series Termination



SYNC_MASTER=J17_TONY SYNC_DATE=03/13/2013

PAGE TITLE
CPU & CHIPSET: SPI and Debug Connector

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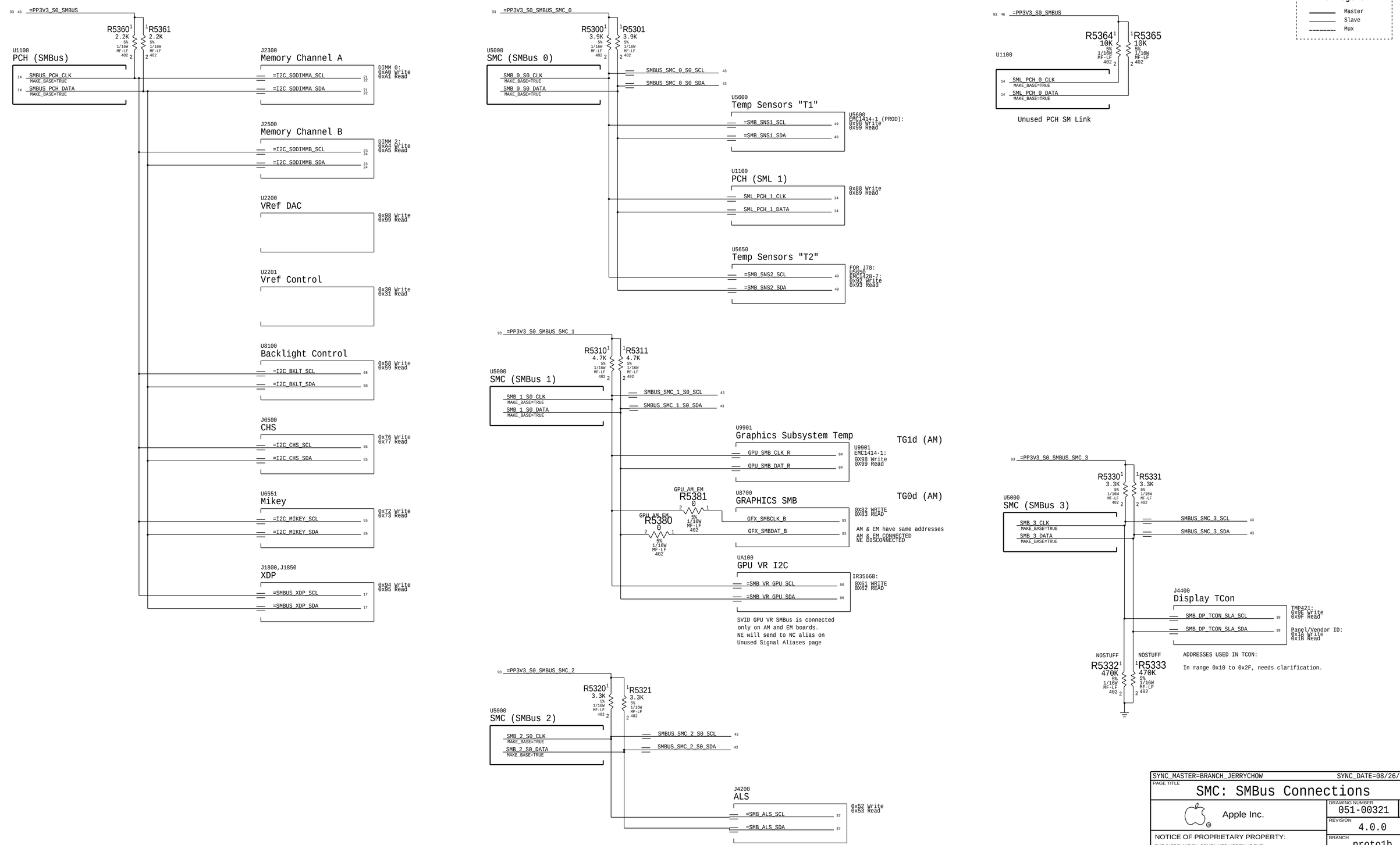

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PAGE TITLE
SMC: SMBus Connections

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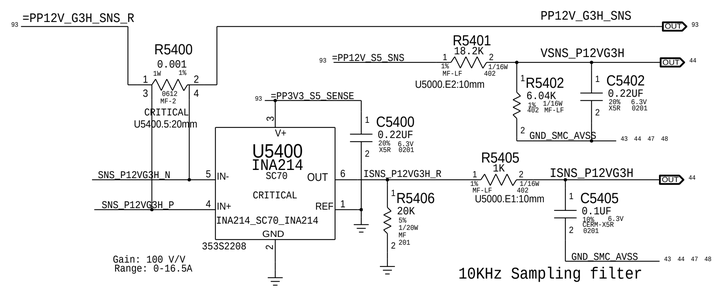
12V G3H (VD2R:ADC0/ID2R:ADC1)

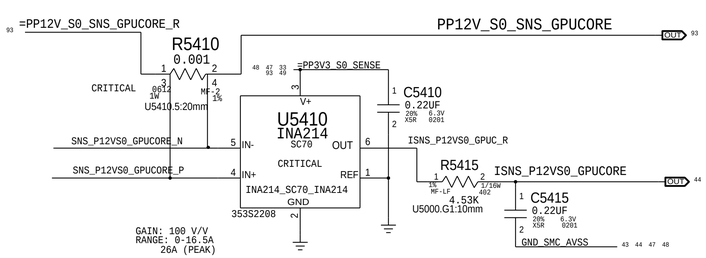
AC/DC lowside sense (System total)



NOTE:VSNS on S5 to avoid burning G3H Power

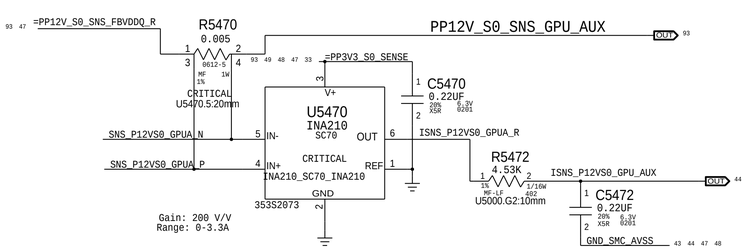
PP12V_S0_GPU (VG1C=VD20, IG1C:ADC17)

GPU highside sense for GPU Core Regulator



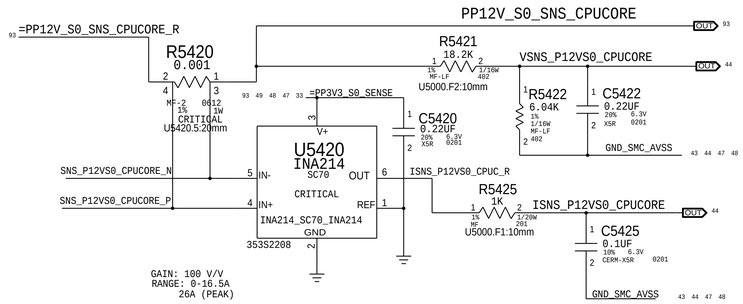
GPU AUX RAILS (VG1A=VD20, IG1A:ADC16)

GPU highside sense for GPU 0.9V & 1.8V VR



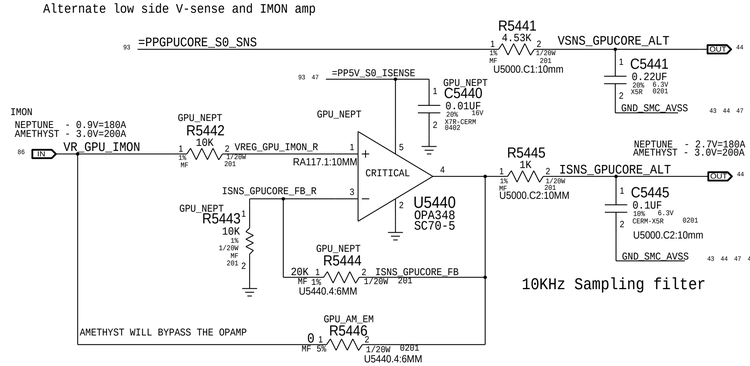
PP12V_S0_CPU (VD20:ADC2 /ID20:ADC3)

CPU highside sense for CPU Core Regulator



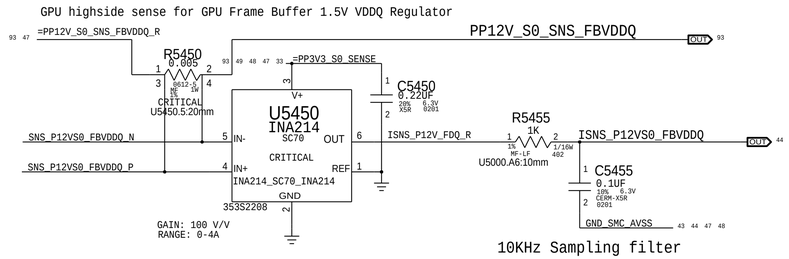
GPU Core - Alt (VG0C:ADC12/IG0C:ADC13)

Alternate low side V-sense and IMON amp

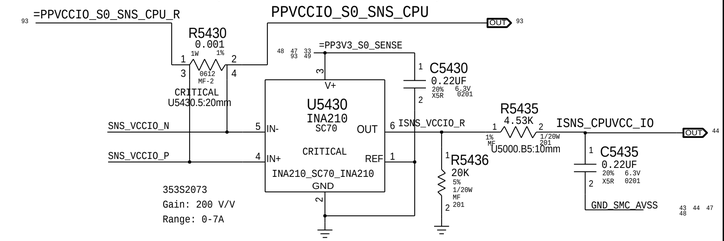


GPU FB (VG1F=VD20, IG1F:ADC11)

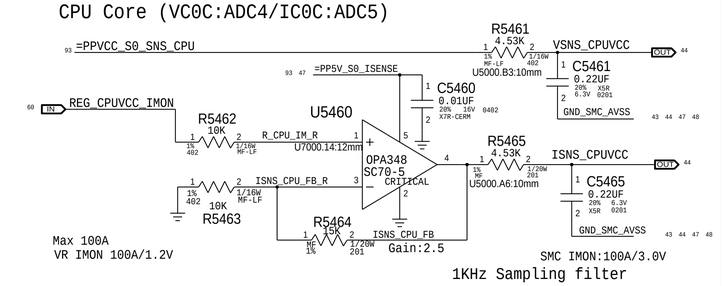
GPU highside sense for GPU Frame Buffer 1.5V VDDQ Regulator



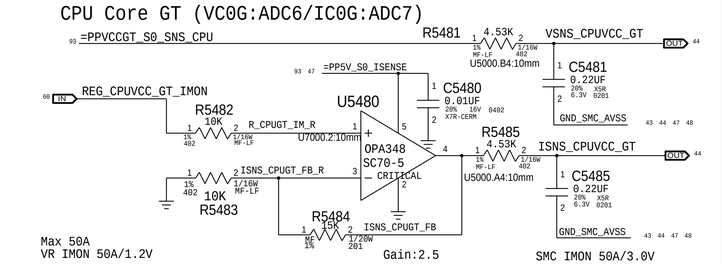
CPU VCCIO (VC0I=tbd, IC0I:ADC8)



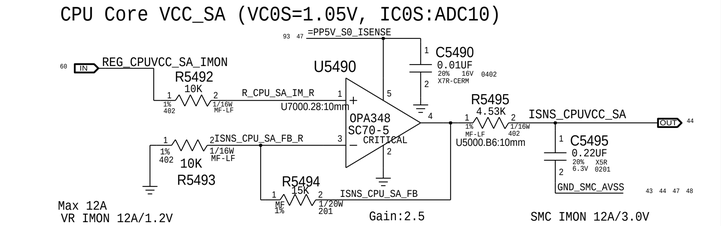
CPU Core (VC0C:ADC4/IC0C:ADC5)



CPU Core GT (VC0G:ADC6/IC0G:ADC7)



CPU Core VCC_SA (VC0S=1.05V, IC0S:ADC10)



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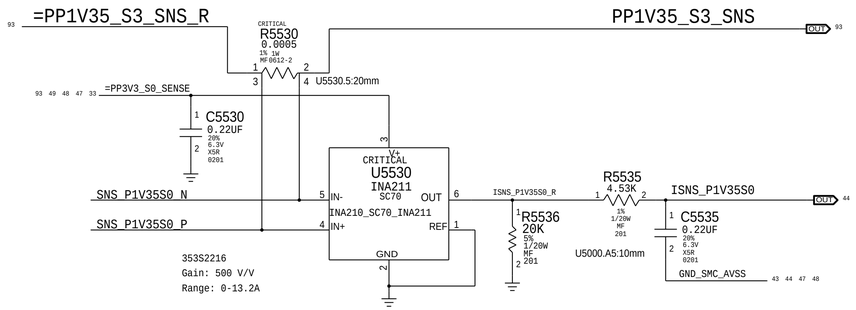
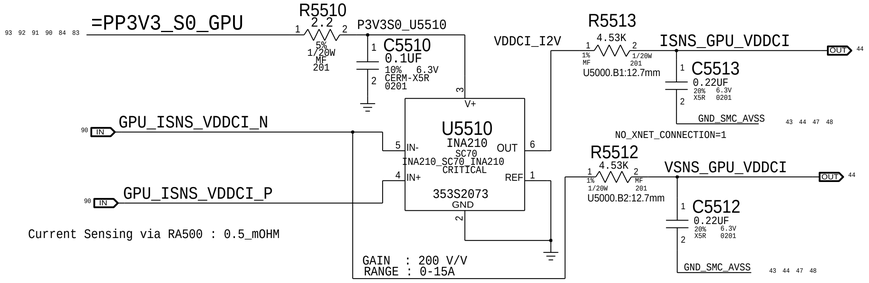
VDDQ S3 (VC0M=VM0R, IC0M:ADC9)

VDDQ lowside sense for SO-DIMM modules

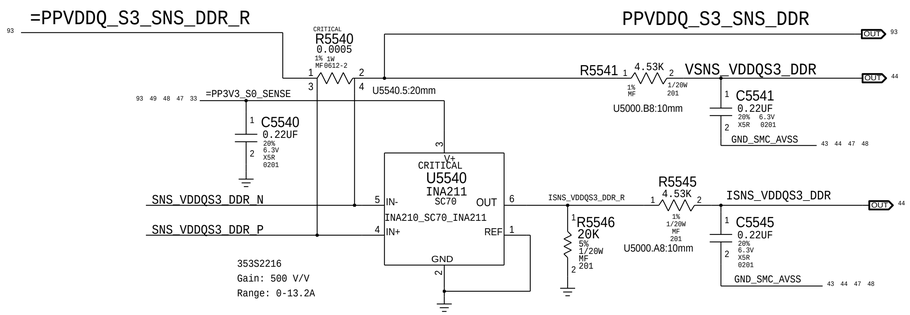


GPU_VDDCI S0 (VG0I:ADC14 /IG0I: ADC15)



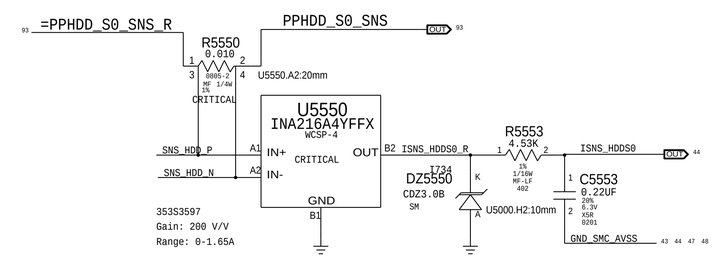
VDDQ S3 (VM0R:ADC22/ IM0R:ADC23)

VDDQ lowside sense for SO-DIMM modules



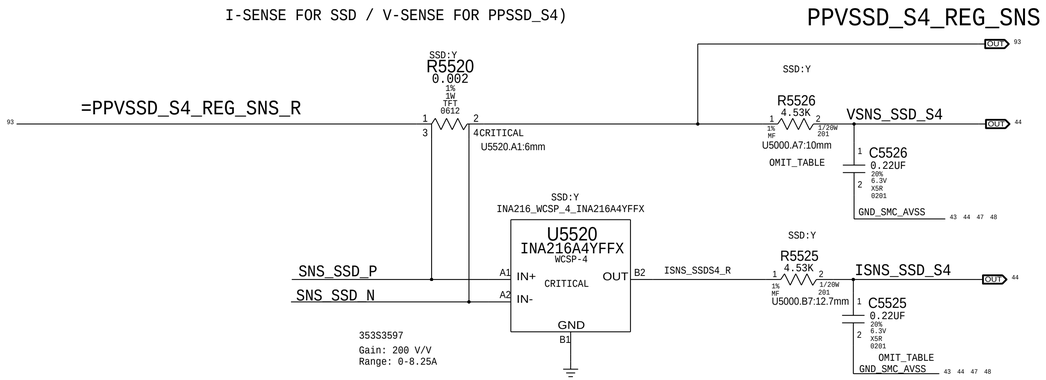
HDD S0 (VH05=5V, IH05:ADC19)

I/V-sense for HDD 5V



SSD S4 (VR1R:ADC20 / IH1R:ADC21)

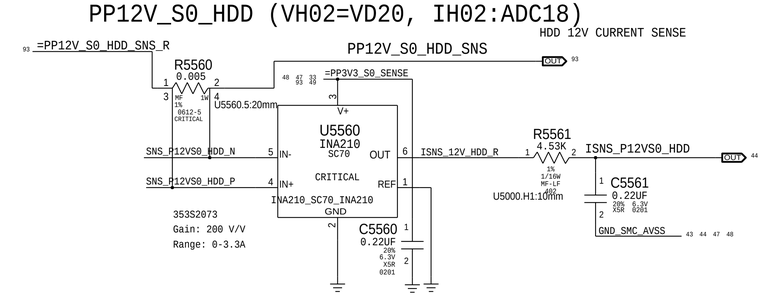
I-SENSE FOR SSD / V-SENSE FOR PPSSD_S4)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0304	2	CAP,0.22UF,201	C5525,C5526	SSD:Y
117S0201	2	RES,0 OHM,201	C5525,C5526	SSD:N

PP12V_S0_HDD (VH02=VD20, IH02:ADC18)

HDD 12V CURRENT SENSE



SYNC_MASTER=BRANCH_JERRYCHOW SYNC_DATE=09/10/2014

PAGE TITLE
SENSORS: I and V Sense(Continued)

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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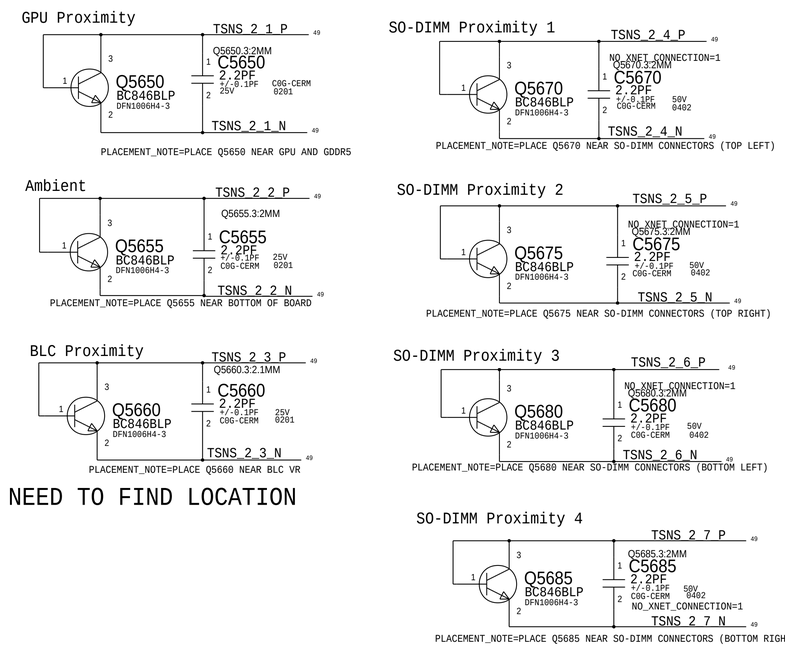
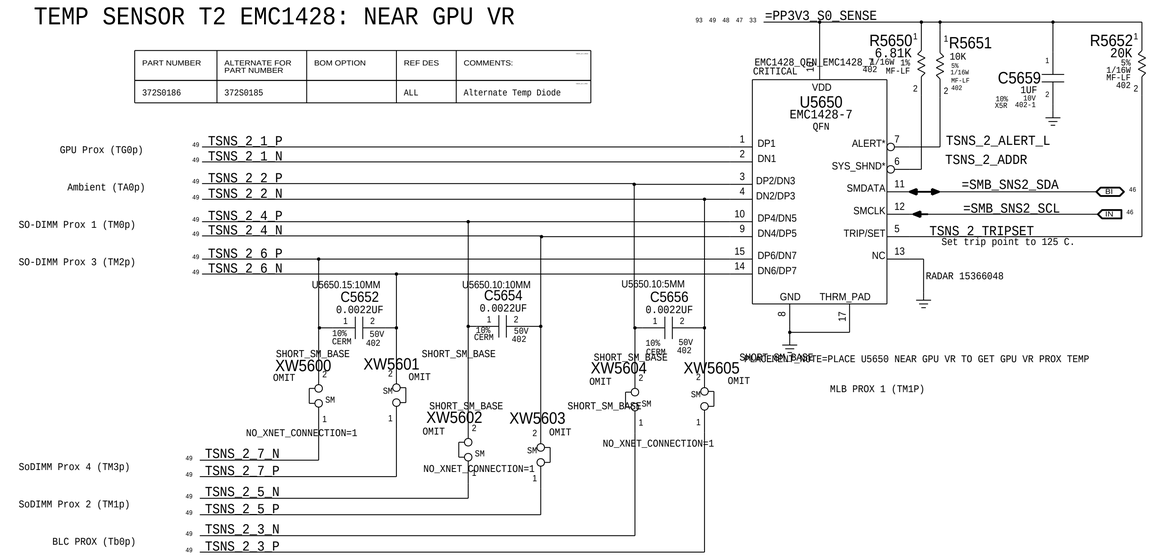


NEED TO FIND LOCATION

TEMP SENSOR T2 EMC1428: NEAR GPU VR

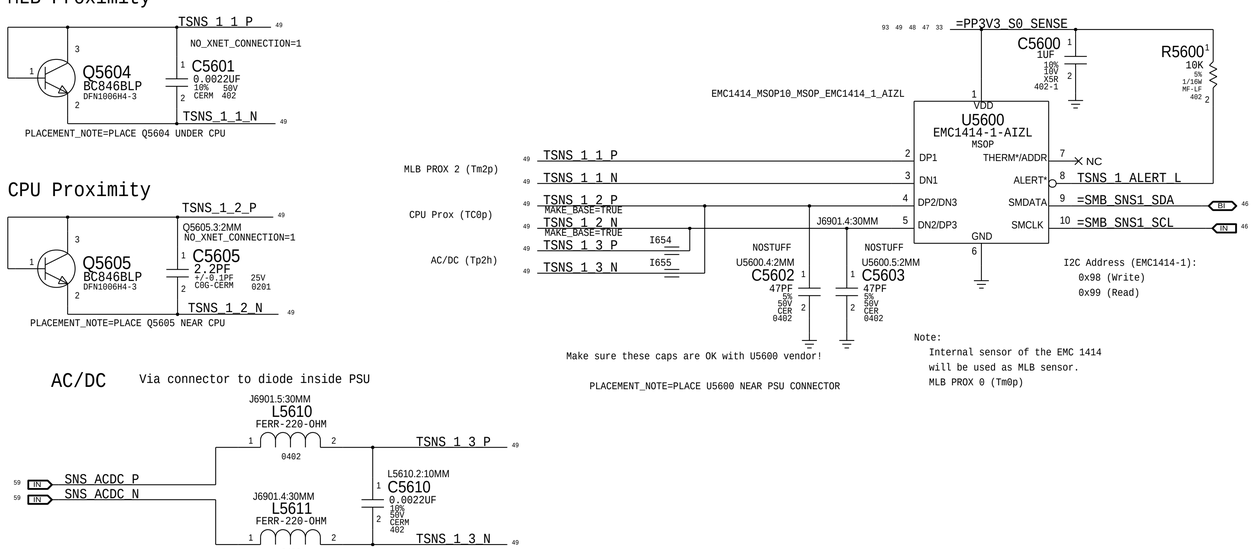
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode

SNS T2: TEMP SENSOR IC



EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

Temperature Sensor T1 EMC1414: Near PSU Conn



SYNC_MASTER=BRANCH_JERRYCHOW SYNC_DATE=09/10/2014

PAGE TITLE
SENSORS: Temperature Sensors

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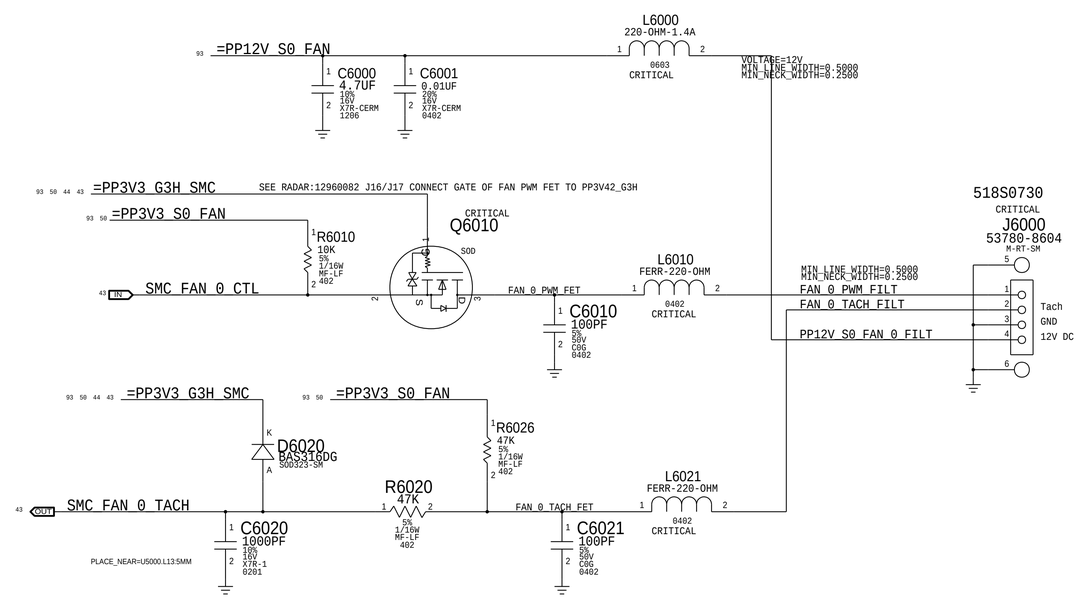
SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).



Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Proto1 Fan Tach instability.

SMC Fan 1 (Unused)

SYNC_MASTER=J16_IG SYNC_DATE=04/29/2013

PAGE TITLE
FAN: System Fan

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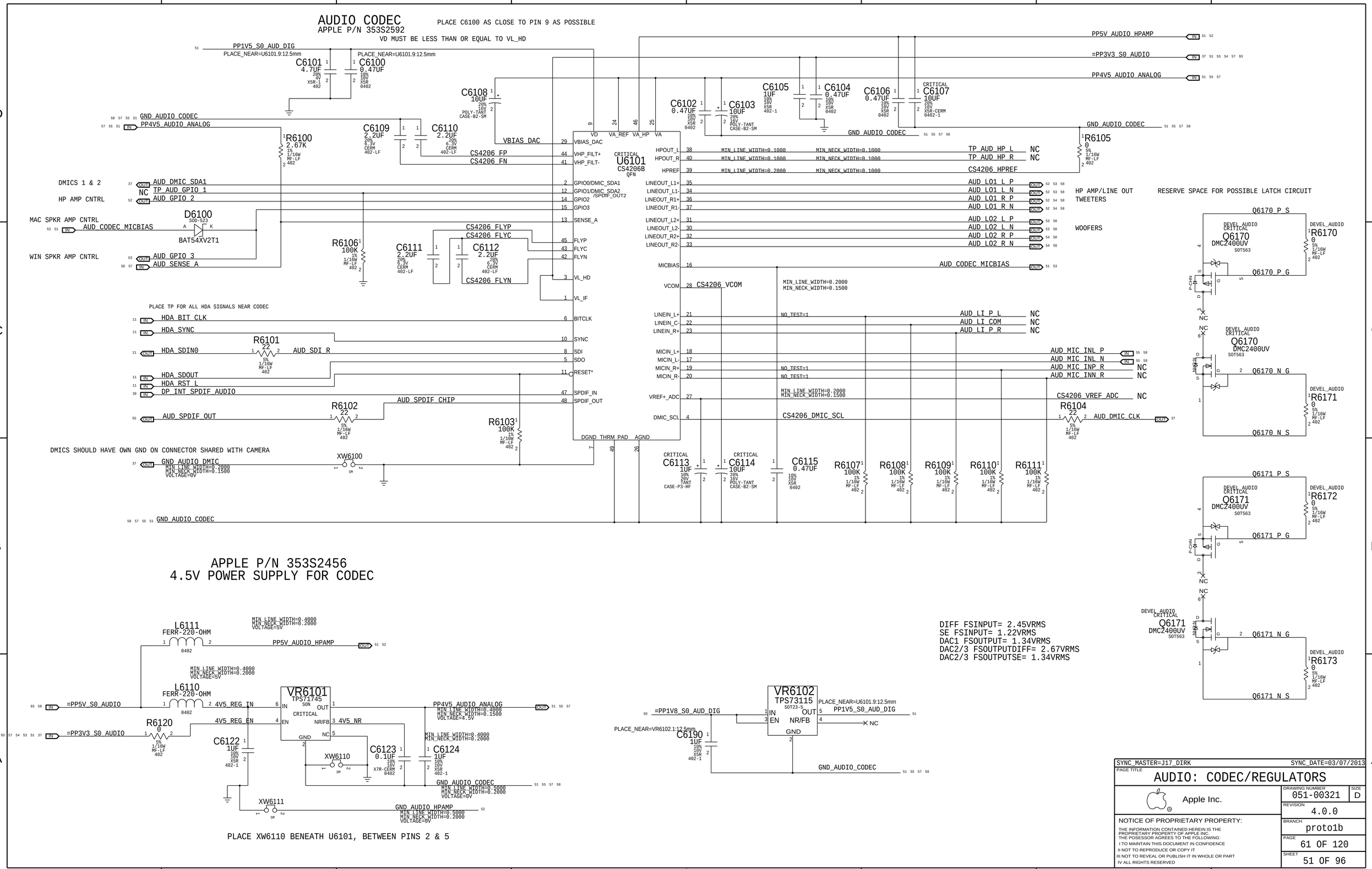

SYNC_MASTER=J17_DIRK SYNC_DATE=03/07/2013

PAGE TITLE
AUDIO: CODEC/REGULATORS

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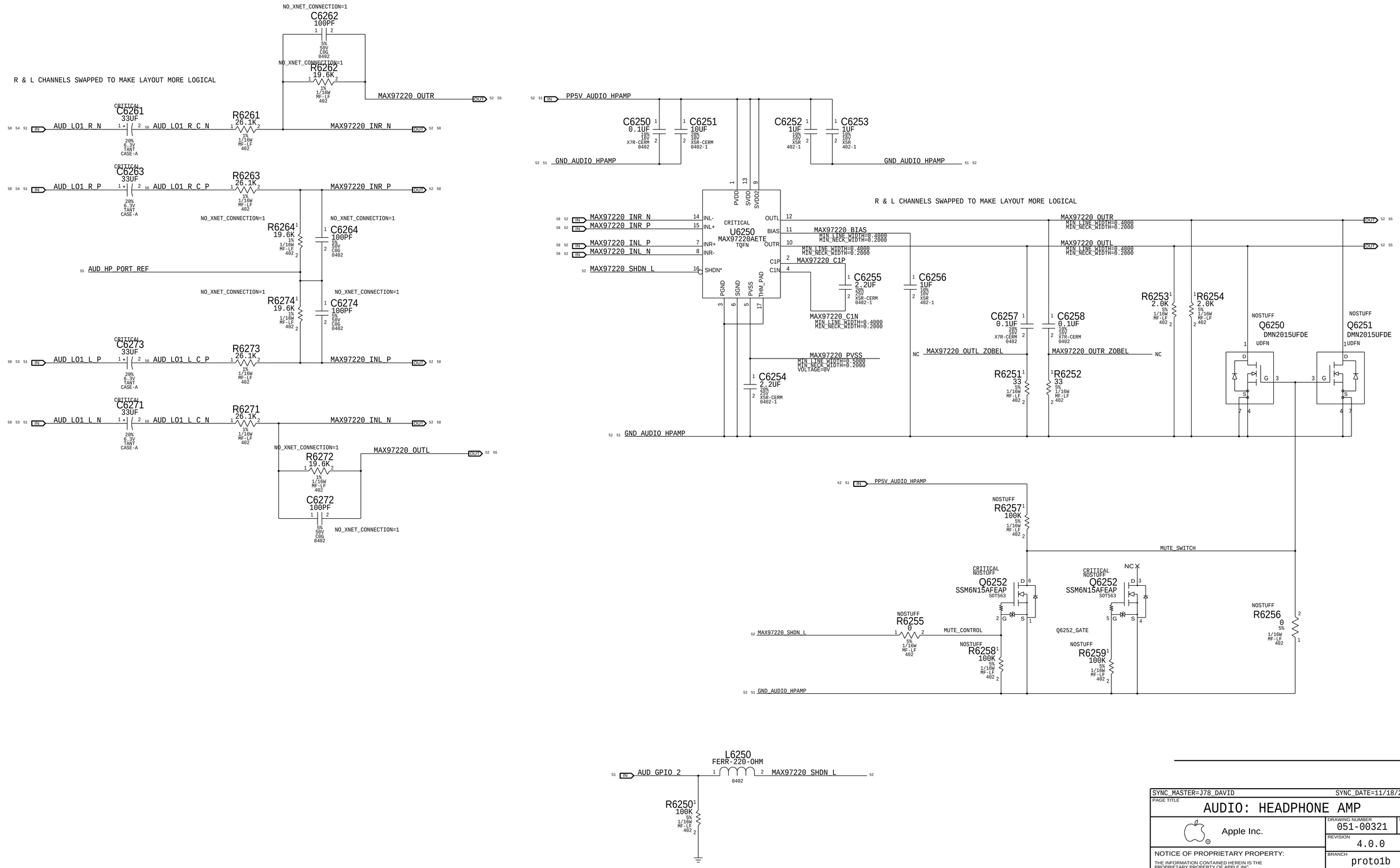

SYNC_MASTER=J78_DAVID SYNC_DATE=11/18/2013

PAGE TITLE

AUDIO: HEADPHONE AMP

Apple Inc.

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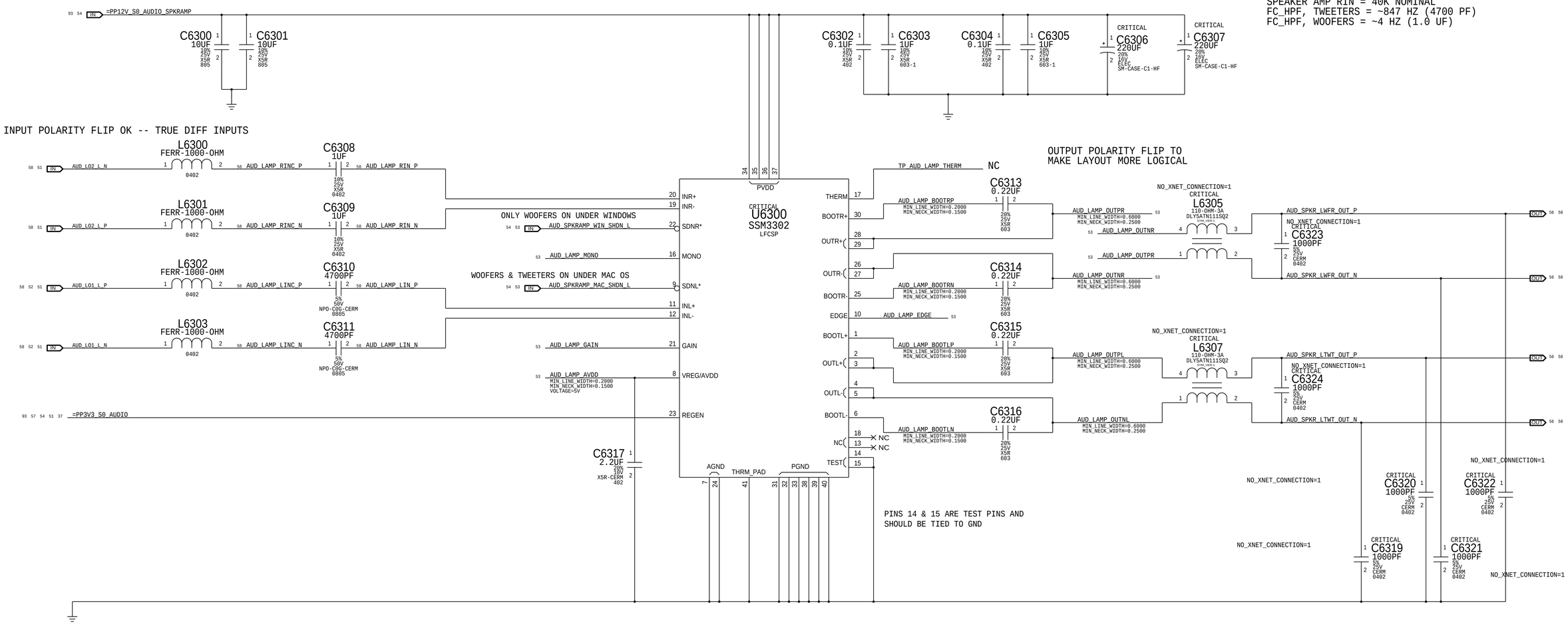
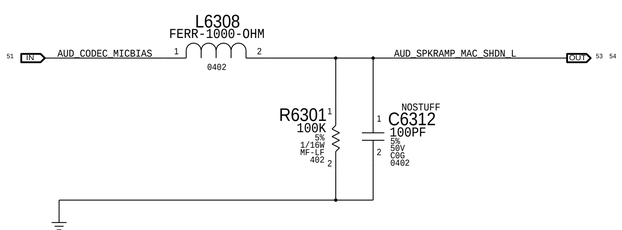
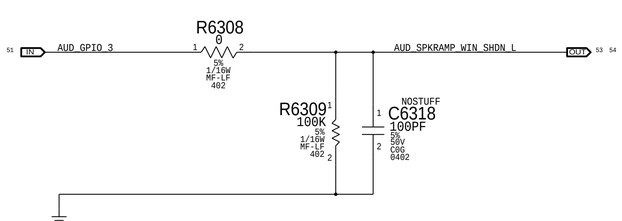
LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +12 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)





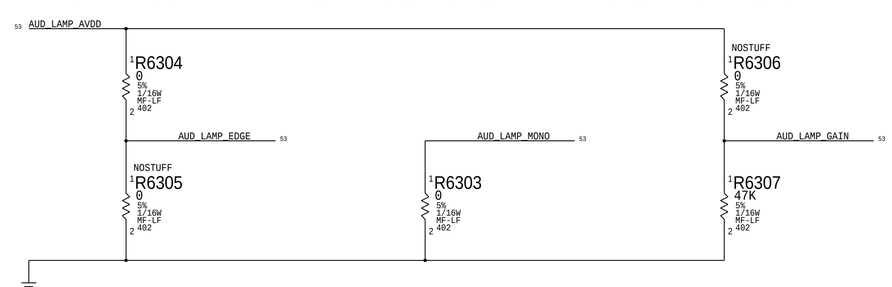


EDGE RATE

CONTROL	R6304	R6305
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6306	R6307
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF



SYNC_MASTER=J78_DAVID SYNC_DATE=11/18/2013

PAGE TITLE
AUDIO: LEFT SPKR AMP

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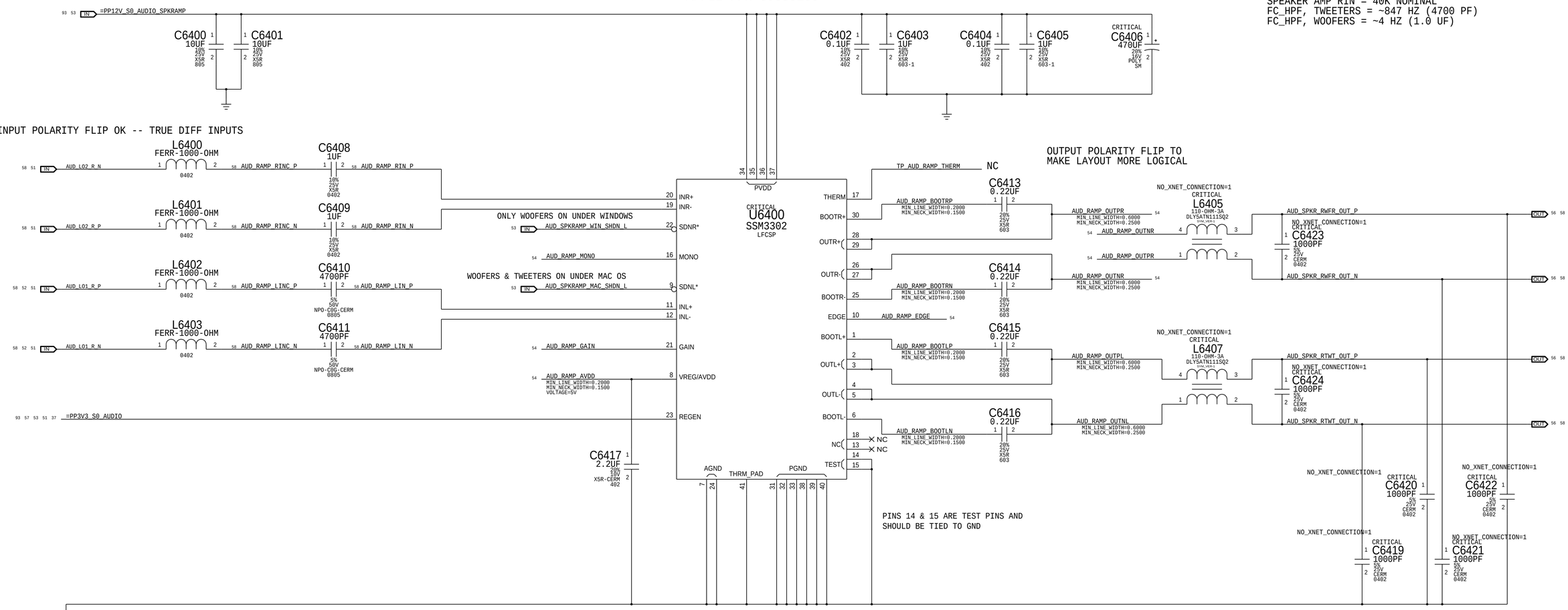
RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +12 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

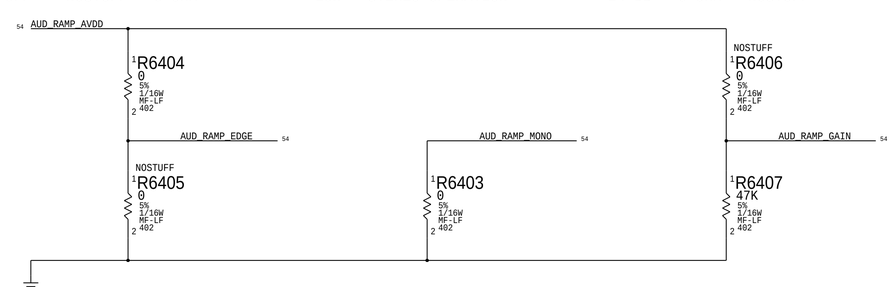


EDGE RATE CONTROL

	R6404	R6405
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6406	R6407
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF



SYNC_MASTER=J78_DAVID SYNC_DATE=11/18/2013

PAGE TITLE
AUDIO: RIGHT SPKR AMP

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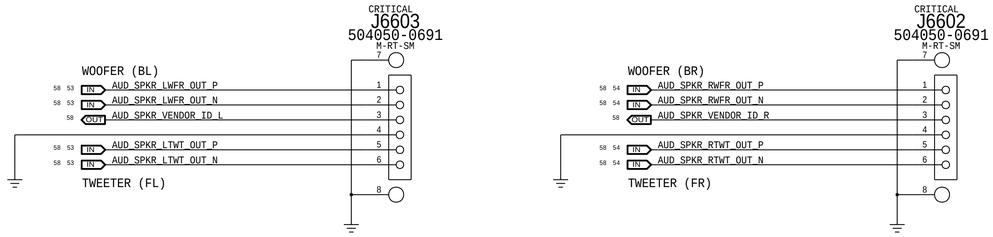
SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862



SYNC_MASTER=J17_DIRK SYNC_DATE=03/07/2013

PAGE TITLE

AUDIO: Spkr/Mic Conn.

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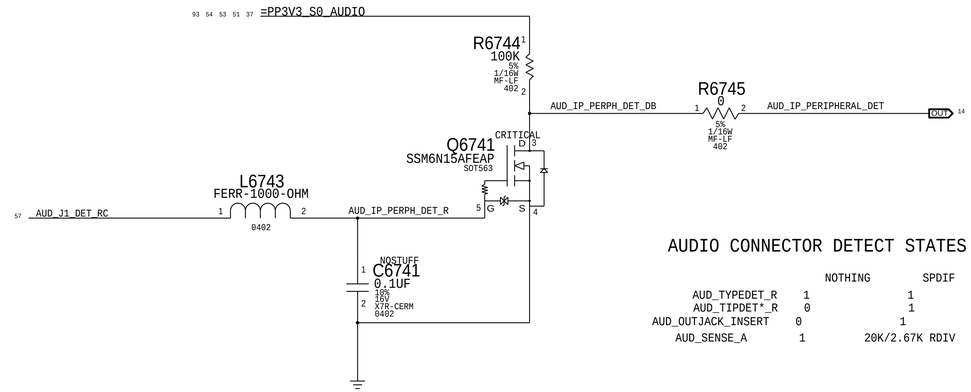
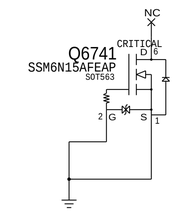
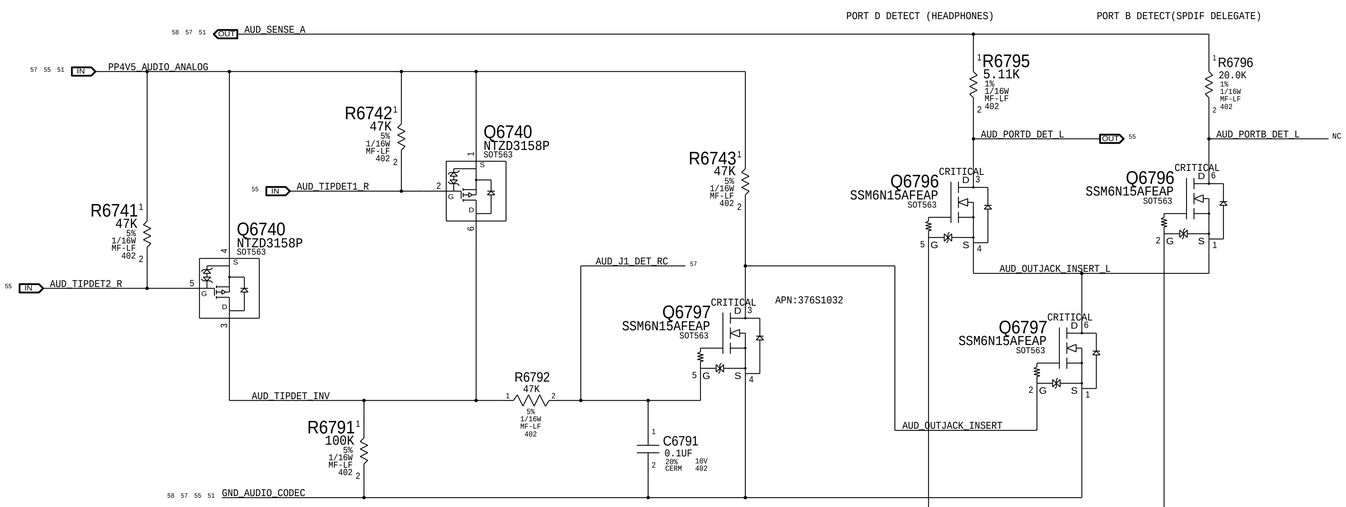
IPHS HS Detect Debounce CKT



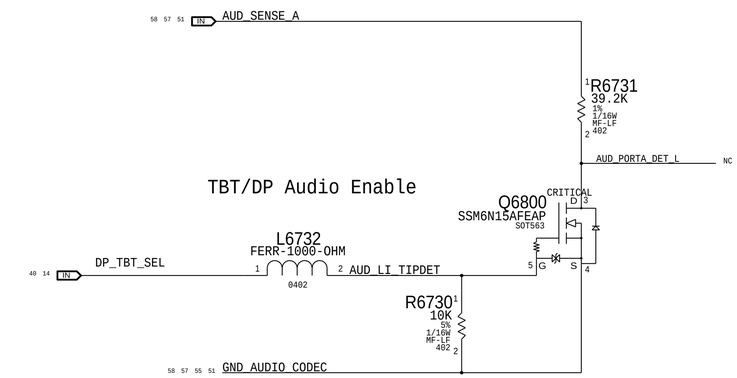
AUDIO CONNECTOR DETECT STATES

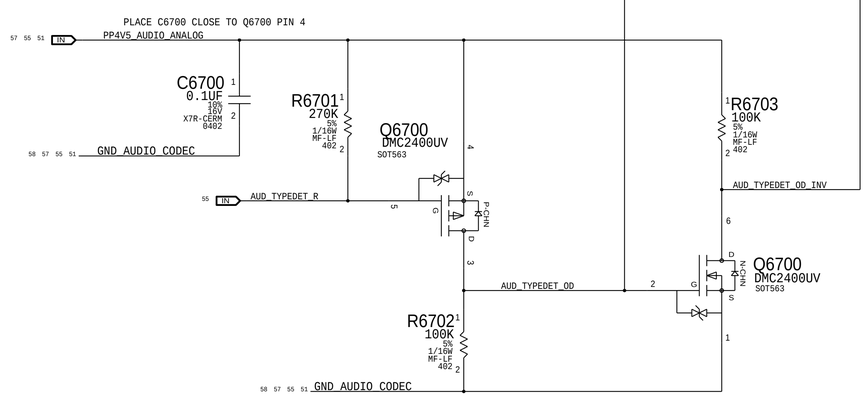
	NOTHING	SPDIF	HEADPHONE
AUD_TYPEDET_R	1	1	0
AUD_TIPDET*_R	0	1	1
AUD_OUTJACK_INSERT	0	1	1
AUD_SENSE_A	1	20K/2.67K RDIV	5.11K/2.67K RDIV





Target Display Mode Detect





SYNC_MASTER=J17_DIRK SYNC_DATE=03/07/2013

PAGE TITLE

AUDIO: Detects/Grounding

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	Lynx POINT GPIO 16	Lynx POINT GPIO 5 (BCVB INT) Lynx POINT GPIO 3 (PERIPH DET)

OTHER DETECT

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

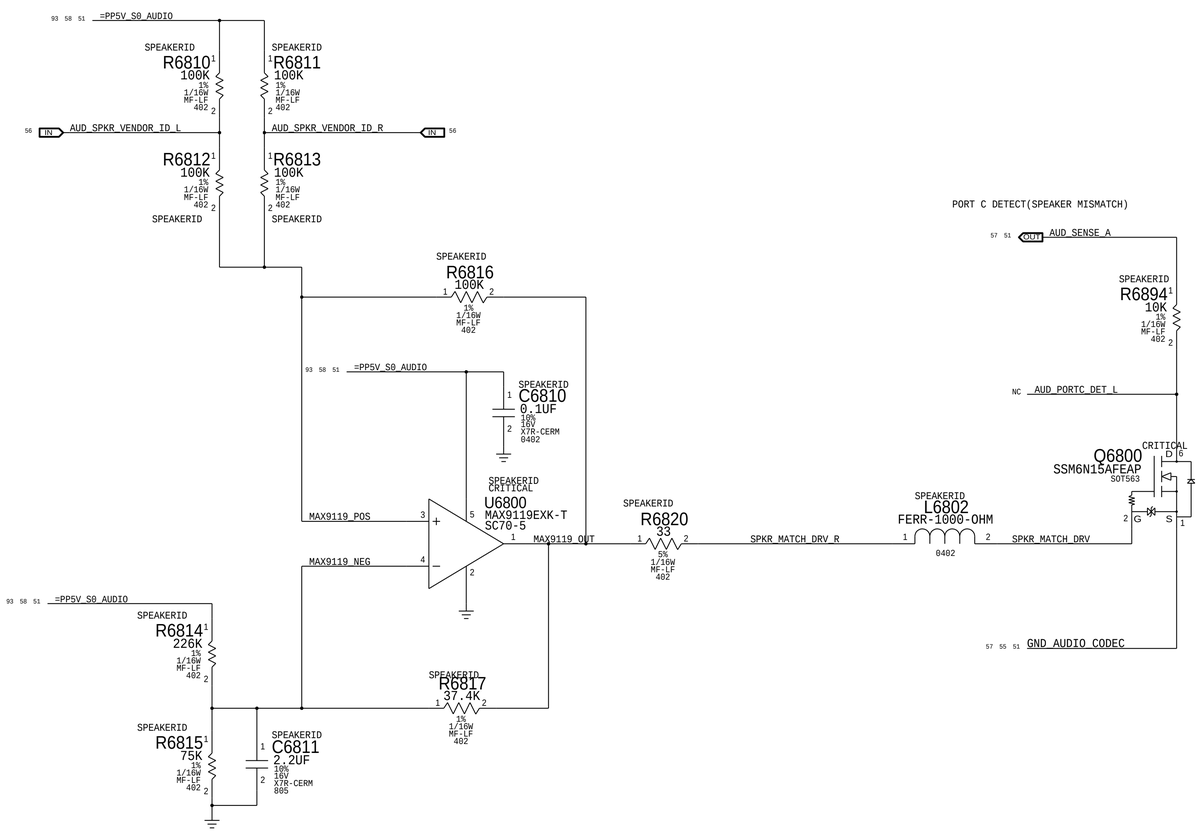
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
P216	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	51 52 53
P215	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	51 52 53
P217	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	52
P218	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	52
P211	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	51 52 54
P212	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	51 52 54
P219	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	52
P220	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	52
P208	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
P206	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
P207	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 54
P204	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 54
P202	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	54
P203	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	54
P229	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	54
P230	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	54
P227	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	54
P221	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	54
P224	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	54
P225	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	54
P226	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	53
P225	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	53
P227	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	53
P228	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	53
P226	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	53
P229	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	53
P204	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	53
P202	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	53
P236	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_P	52
P238	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_N	52
P237	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_P	52
P239	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_N	52
P240	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	54 56
P241	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	54 56
P242	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	54 56
P243	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	54 56
P244	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	53 56
P245	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	53 56
P246	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	53 56
P247	SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	53 56
P328	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	51 55
P327	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	51 55
P328	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_P	55
P326	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_N	55
P324	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P	55
P325	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N	55
P324	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_P	55
P325	AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_N	55

CIRCUIT THEORY OF OPERATION AVAILABLE IN <RDAR://PROBLEM/9776522>



PORT C DETECT(SPEAKER MISMATCH)

SYNC_MASTER=J78_DAVID	SYNC_DATE=11/21/2013
PAGE TITLE	AUDIO: Speaker ID
Apple Inc.	DRAWING NUMBER 051-00321 SIZE D
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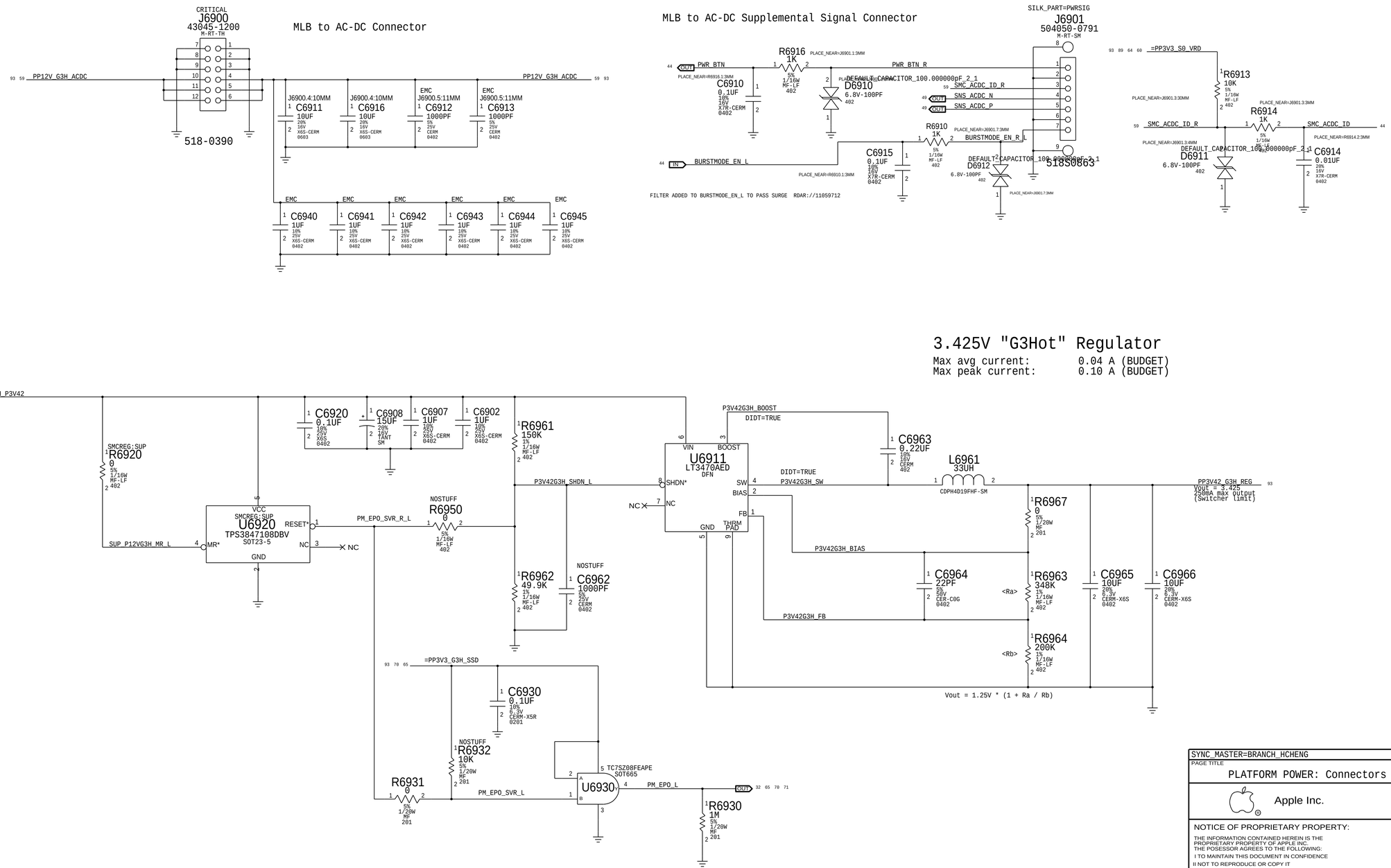

SYNC_MASTER=BRANCH_HCHENG SYNC_DATE=10/29/2014

PAGE TITLE

PLATFORM POWER: Connectors / VReg G3Hot

Apple Inc.

DRAWING NUMBER	051-00321
SIZE	D
REVISION	4.0.0
BRANCH	proto1b
PAGE	69 OF 120
SHEET	59 OF 96

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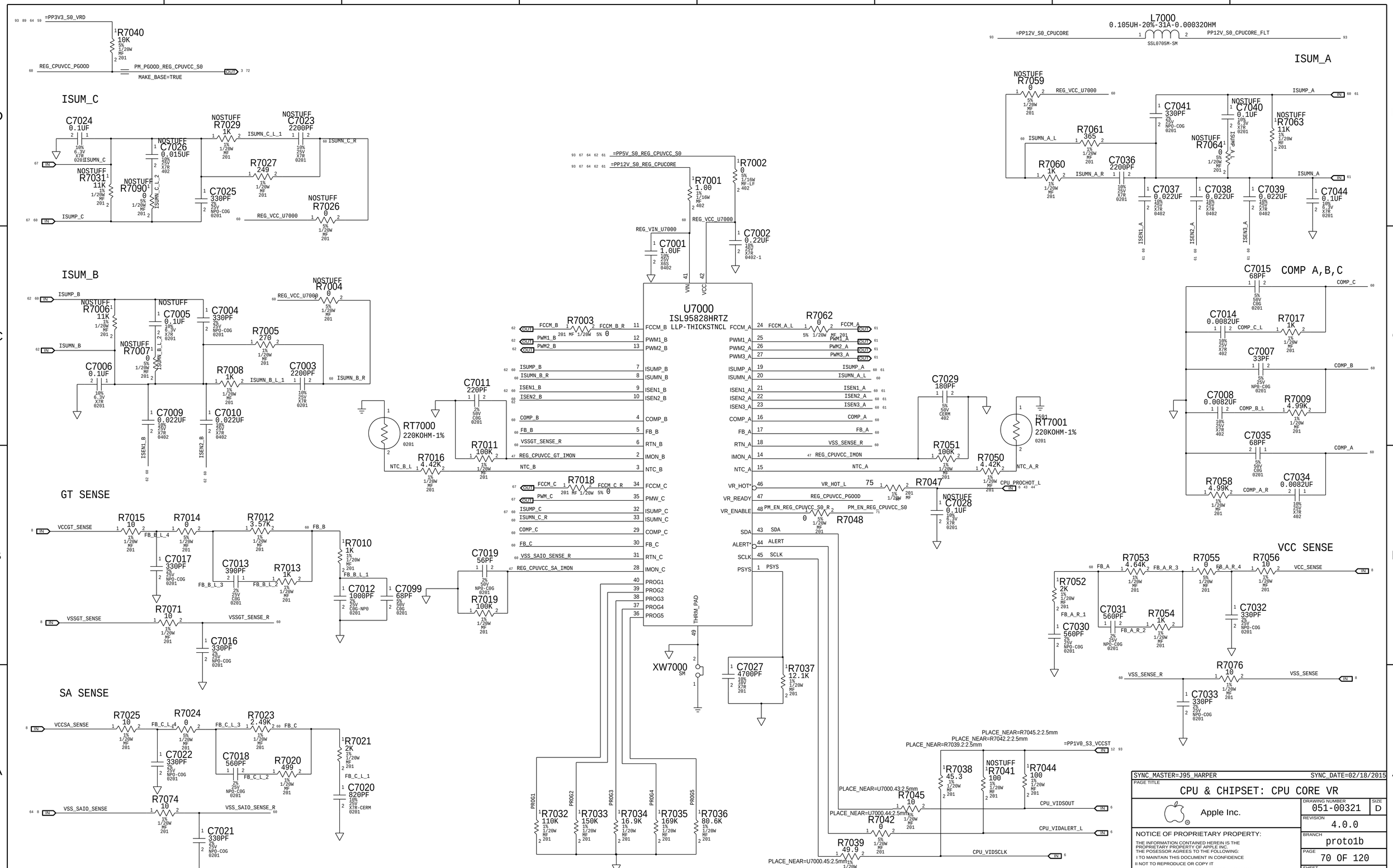

SYNC_MASTER=J95_HARPER SYNC_DATE=02/18/2015

PAGE TITLE: CPU & CHIPSET: CPU CORE VR

Apple Inc.

DRAWING NUMBER: 051-00321 SIZE: D

REVISION: 4.0.0

BRANCH: proto1b

PAGE: 70 OF 120

SHEET: 60 OF 96

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CPU VCC Regulator
EDC = 100A
TDC = 70A

CPU VCORE Phase 1

=PP12V_S0_REG_CPUCORE
=PP5V_S0_REG_CPUVCC_S0
PP5V_S0_VRD_VCIN_A1
R7127 1 5% 1/16W MF-LF 402
C7128 1UF 10% 25V X6S-CERM 0402
C7111 10UF 20% 16V X6S-CERM 0603
R7129 10K 5% 1/16W MF-LF 402
NOSTUFF R7128 10K 5% 1/16W MF-LF 402
Q7110 SIC625CD MLP-THICKSTNCL
VIN0 VIN1 VCIN VDRV ZCD_EN* DSBL* PWM THWN BOOT PHASE VSWH0 VSWH1 GH GL0 GL1 CGND CGND PGND PGND
FCCM_A
DSBL_A_1
PWM1_A
THWN_A_1
BOOST_A_1
PHASE_A_1
BOOST_A_1_RC
R7116 0 5% 1/10W MF-LF 603
C7116 0.22UF 10% 25V X7R 0402-1
NOSTUFF C7197 15UF 20% 16V TANT SM
CRITICAL C7126 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7125 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7196 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7129 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7112 1UF 10% 25V X6S-CERM 0402
CRITICAL C7113 1UF 10% 25V X6S-CERM 0402
CRITICAL C7118 1UF 10% 25V X6S-CERM 0402
CRITICAL C7119 1UF 10% 25V X6S-CERM 0402
CRITICAL C7120 1UF 10% 25V X6S-CERM 0402
CRITICAL C7121 1UF 10% 25V X6S-CERM 0402
EMC CRITICAL C7114 1UF 10% 25V X6S-CERM 0402
EMC CRITICAL C7115 1UF 10% 25V X6S-CERM 0402
SW_A_1
CRITICAL L7110 0.22UH-20%-43A-0.00060HM PIME104T-SM
PPCPUVCC_S0_SENSE_1_1
CRITICAL R7110 0.0005 1% 1W MF 0612-2
REG_CPUVCC_ISNS_1_P
REG_CPUVCC_ISNS_1_N
R7118 3.9 1% 1/20W MF 201
NO_XNET_CONNECTION=1
ISUMN_A
NOSTUFF C7117 0.001UF 10% 50V X7R-CERM 0402
REG_SNUBBER_CPUVCC_1
NOSTUFF R7117 2.2 5% 1/10W MF-LF 805
R7119 1K 1% 1/20W MF 201
R7120 100K 1% 1/20W MF 201
R7121 100K 1% 1/20W MF 201
REG_CPUVCC_ISNS_2_N
R7122 100K 1% 1/20W MF 201
REG_CPUVCC_ISNS_3_N
ISEN1_A
ISUMP_A
PPVCC_S0_CPU_REG
C7122 10UF 20% 4V X6S-CERM 0402-1
C7123 10UF 20% 4V X6S-CERM 0402-1
C7190 10UF 20% 4V X6S-CERM 0402-1
C7191 10UF 20% 4V X6S-CERM 0402-1

CPU VCORE Phase 2

=PP12V_S0_REG_CPUCORE
=PP5V_S0_REG_CPUVCC_S0
PP5V_S0_VRD_VCIN_A2
R7147 1 5% 1/16W MF-LF 402
C7148 1UF 10% 25V X6S-CERM 0402
C7147 10UF 20% 16V X6S-CERM 0603
R7149 10K 5% 1/16W MF-LF 402
NOSTUFF R7148 10K 5% 1/16W MF-LF 402
Q7130 SIC625CD MLP-THICKSTNCL
VIN0 VIN1 VCIN VDRV ZCD_EN* DSBL* PWM THWN BOOT PHASE VSWH0 VSWH1 GH GL0 GL1 CGND CGND PGND PGND
FCCM_A
DSBL_A_2
PWM2_A
THWN_A_2
BOOST_A_2
PHASE_A_2
BOOST_A_2_RC
R7136 0 5% 1/10W MF-LF 603
C7136 0.22UF 10% 25V X7R 0402-1
NOSTUFF C7198 15UF 20% 16V TANT SM
CRITICAL C7144 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7145 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7146 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7130 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7132 1UF 10% 25V X6S-CERM 0402
CRITICAL C7133 1UF 10% 25V X6S-CERM 0402
CRITICAL C7138 1UF 10% 25V X6S-CERM 0402
CRITICAL C7139 1UF 10% 25V X6S-CERM 0402
CRITICAL C7140 1UF 10% 25V X6S-CERM 0402
CRITICAL C7141 1UF 10% 25V X6S-CERM 0402
EMC CRITICAL C7134 1UF 10% 25V X6S-CERM 0402
EMC CRITICAL C7131 1UF 10% 25V X6S-CERM 0402
SW_A_2
CRITICAL L7130 0.22UH-20%-43A-0.00060HM PIME104T-SM
PPCPUVCC_S0_SENSE_2_1
CRITICAL R7130 0.0005 1% 1W MF 0612-2
REG_CPUVCC_ISNS_2_P
REG_CPUVCC_ISNS_2_N
R7138 3.9 1% 1/20W MF 201
NO_XNET_CONNECTION=1
ISUMN_A
NOSTUFF C7137 0.001UF 10% 50V X7R-CERM 0402
REG_SNUBBER_CPUVCC_2
NOSTUFF R7137 2.2 5% 1/10W MF-LF 805
R7139 1K 1% 1/20W MF 201
R7140 100K 1% 1/20W MF 201
R7141 100K 1% 1/20W MF 201
REG_CPUVCC_ISNS_1_N
R7142 100K 1% 1/20W MF 201
REG_CPUVCC_ISNS_3_N
ISEN2_A
ISUMP_A
PPVCC_S0_CPU_REG
C7142 10UF 20% 4V X6S-CERM 0402-1
C7143 10UF 20% 4V X6S-CERM 0402-1
C7192 10UF 20% 4V X6S-CERM 0402-1
C7193 10UF 20% 4V X6S-CERM 0402-1

CPU Phase 3

=PP12V_S0_REG_CPUCORE
=PP5V_S0_REG_CPUVCC_S0
PP5V_S0_VRD_VCIN_A3
R7167 1 5% 1/16W MF-LF 402
C7168 1UF 10% 25V X6S-CERM 0402
C7167 10UF 20% 16V X6S-CERM 0603
R7169 10K 5% 1/16W MF-LF 402
NOSTUFF R7168 10K 5% 1/16W MF-LF 402
Q7150 SIC625CD MLP-THICKSTNCL
VIN0 VIN1 VCIN VDRV ZCD_EN* DSBL* PWM THWN BOOT PHASE VSWH0 VSWH1 GH GL0 GL1 CGND CGND PGND PGND
FCCM_A
DSBL_A_3
PWM3_A
THWN_A_3
BOOST_A_3
PHASE_A_3
BOOST_A_3_RC
R7156 0 5% 1/10W MF-LF 603
C7156 0.22UF 10% 25V X7R 0402-1
NOSTUFF C7199 15UF 20% 16V TANT SM
CRITICAL C7172 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7171 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7170 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7150 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C7152 1UF 10% 25V X6S-CERM 0402
CRITICAL C7153 1UF 10% 25V X6S-CERM 0402
CRITICAL C7161 1UF 10% 25V X6S-CERM 0402
CRITICAL C7158 1UF 10% 25V X6S-CERM 0402
CRITICAL C7159 1UF 10% 25V X6S-CERM 0402
CRITICAL C7160 1UF 10% 25V X6S-CERM 0402
EMC CRITICAL C7154 1UF 10% 25V X6S-CERM 0402
EMC CRITICAL C7155 1UF 10% 25V X6S-CERM 0402
SW_A_3
CRITICAL L7150 0.22UH-20%-43A-0.00060HM PIME104T-SM
PPCPUVCC_S0_SENSE_3_1
CRITICAL R7150 0.0005 1% 1W MF 0612-2
REG_CPUVCC_ISNS_3_P
REG_CPUVCC_ISNS_3_N
R7158 3.9 1% 1/20W MF 201
NO_XNET_CONNECTION=1
ISUMN_A
NOSTUFF C7157 0.001UF 10% 50V X7R-CERM 0402
REG_SNUBBER_CPUVCC_3
NOSTUFF R7157 2.2 5% 1/10W MF-LF 805
R7159 1K 1% 1/20W MF 201
R7160 100K 1% 1/20W MF 201
R7161 100K 1% 1/20W MF 201
REG_CPUVCC_ISNS_1_N
R7162 100K 1% 1/20W MF 201
REG_CPUVCC_ISNS_2_N
ISEN3_A
ISUMP_A
PPVCC_S0_CPU_REG
C7194 10UF 20% 4V X6S-CERM 0402-1
C7173 10UF 20% 4V X6S-CERM 0402-1
C7162 10UF 20% 4V X6S-CERM 0402-1
C7163 10UF 20% 4V X6S-CERM 0402-1

CPU VCORE OUTPUT DECOUPLING

PPVCC_S0_CPU_REG
NOSTUFF CRITICAL C7180 470UF-0.00450HM 20% 2.5V POLY-TANT SM
CRITICAL C7181 470UF-0.00450HM 20% 2.5V POLY-TANT SM
CRITICAL C7182 470UF-0.00450HM 20% 2.5V POLY-TANT SM
NOSTUFF CRITICAL C7183 470UF-0.00450HM 20% 2.5V POLY-TANT SM
CRITICAL C7184 470UF-0.00450HM 20% 2.5V POLY-TANT SM
CRITICAL C7185 470UF-0.00450HM 20% 2.5V POLY-TANT SM

DRAWING: LAST_MODIFIED=Thu Feb 26 18:42:55 2015
SYNC_MASTER=J95_HCHENG SYNC_DATE=02/24/2015
PAGE TITLE: CPU & CHIPSET: CPU CORE VR (VCC)
Apple Inc.
DRAWING NUMBER: 051-00321 SIZE: D
REVISION: 4.0.0
BRANCH: proto1b
PAGE: 71 OF 120
SHEET: 61 OF 96

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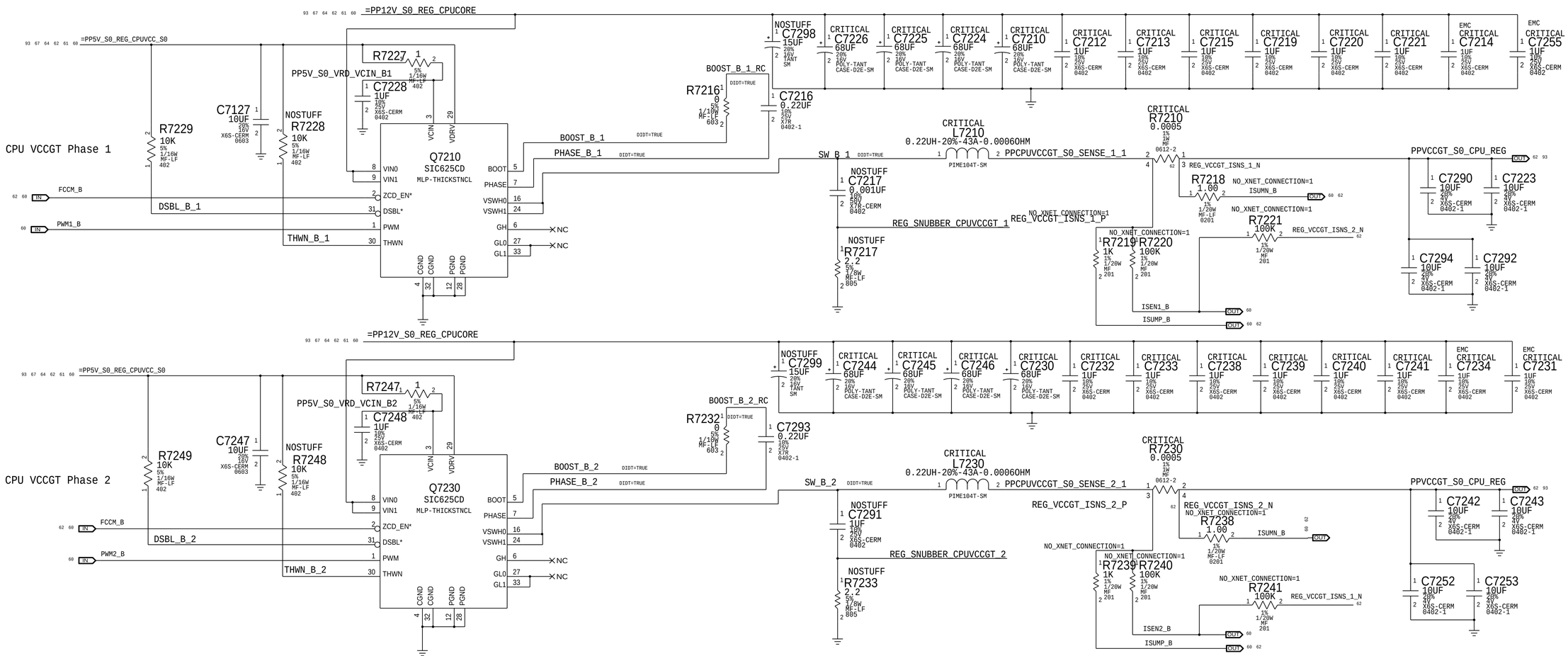
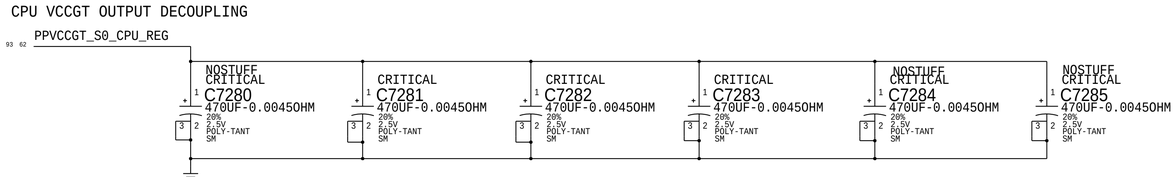
CPU VCCGT Regulator

EDC = 51A

TDC = 37A



CPU VCCGT OUTPUT DECOUPLING



DRAWING	LAST_MODIFIED=Thu Feb 26 18:42:55 2015
SYNC_MASTER=J95_HCHENG	SYNC_DATE=02/24/2015
PAGE TITLE	CPU & CHIPSET: CPU CORE VR (VCCGT)
Apple Inc.	DRAWING NUMBER 051-00321 · SIZE D
	REVISION 4.0.0
	BRANCH proto1b
	PAGE 72 OF 120
	SHEET 62 OF 96

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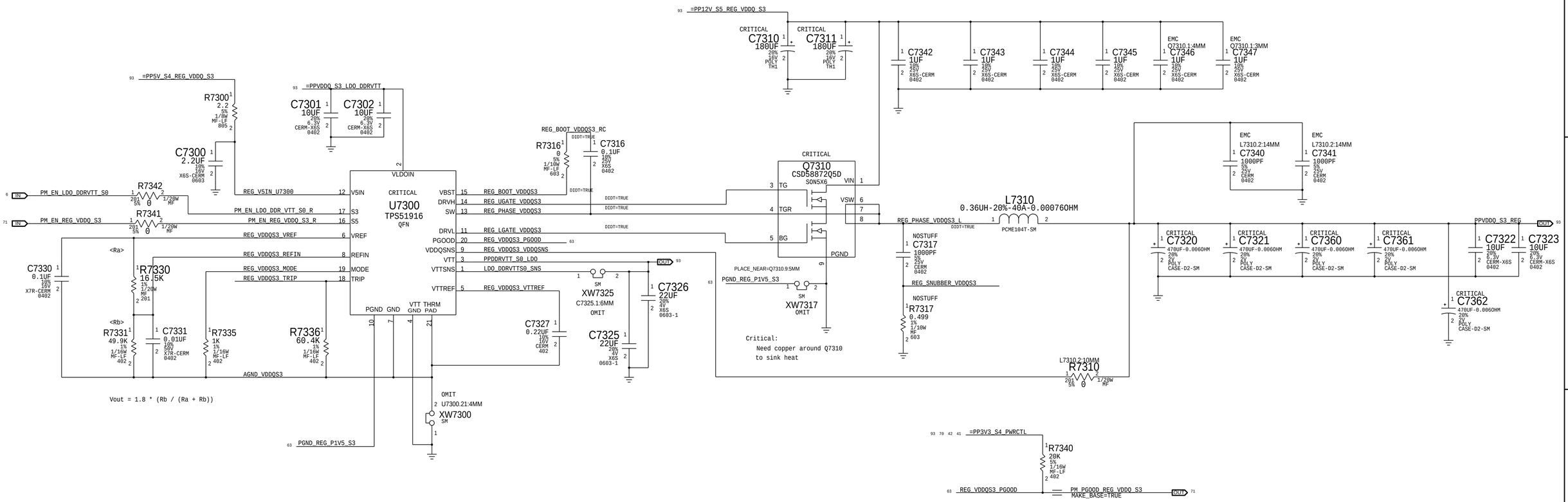
VDDQ (1.35V) S3 REGULATOR

EDC = 20A

TDC = 14A



SYNC_MASTER=BRANCH_HCHENG SYNC_DATE=10/29/2014

PAGE TITLE
CPU & CHIPSET: CPU VDDQ VR

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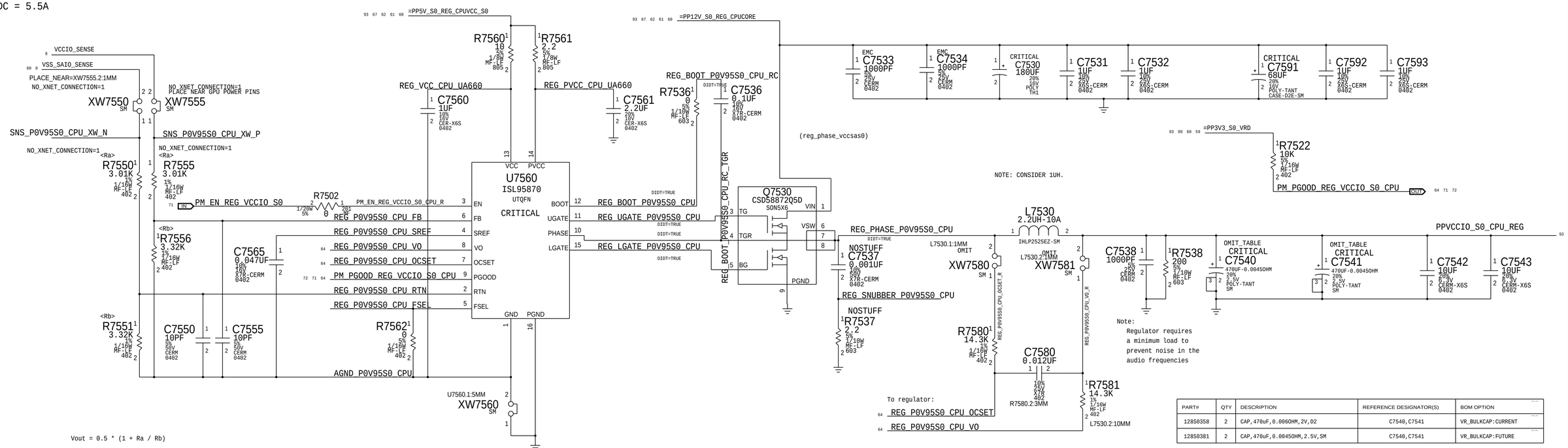
VCCIO (0.95V) S0 REGULATOR

EDC = 5.5A

TDC = 5.5A



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0358	2	CAP,470uF,0.0060HM,2V,D2	C7540,C7541	VR_BULKCAP:CURRENT
128S0381	2	CAP,470uF,0.0045OHM,2.5V,SM	C7540,C7541	VR_BULKCAP:FUTURE

DRAWING LAST_MODIFIED=Thu Feb 26 18:42:55 2015

SYNC_MASTER=J95_HARPER SYNC_DATE=02/13/2015

PAGE TITLE

CPU & CHIPSET: CPU VCCIO VR

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DRAWING NUMBER 051-00321 SIZE D

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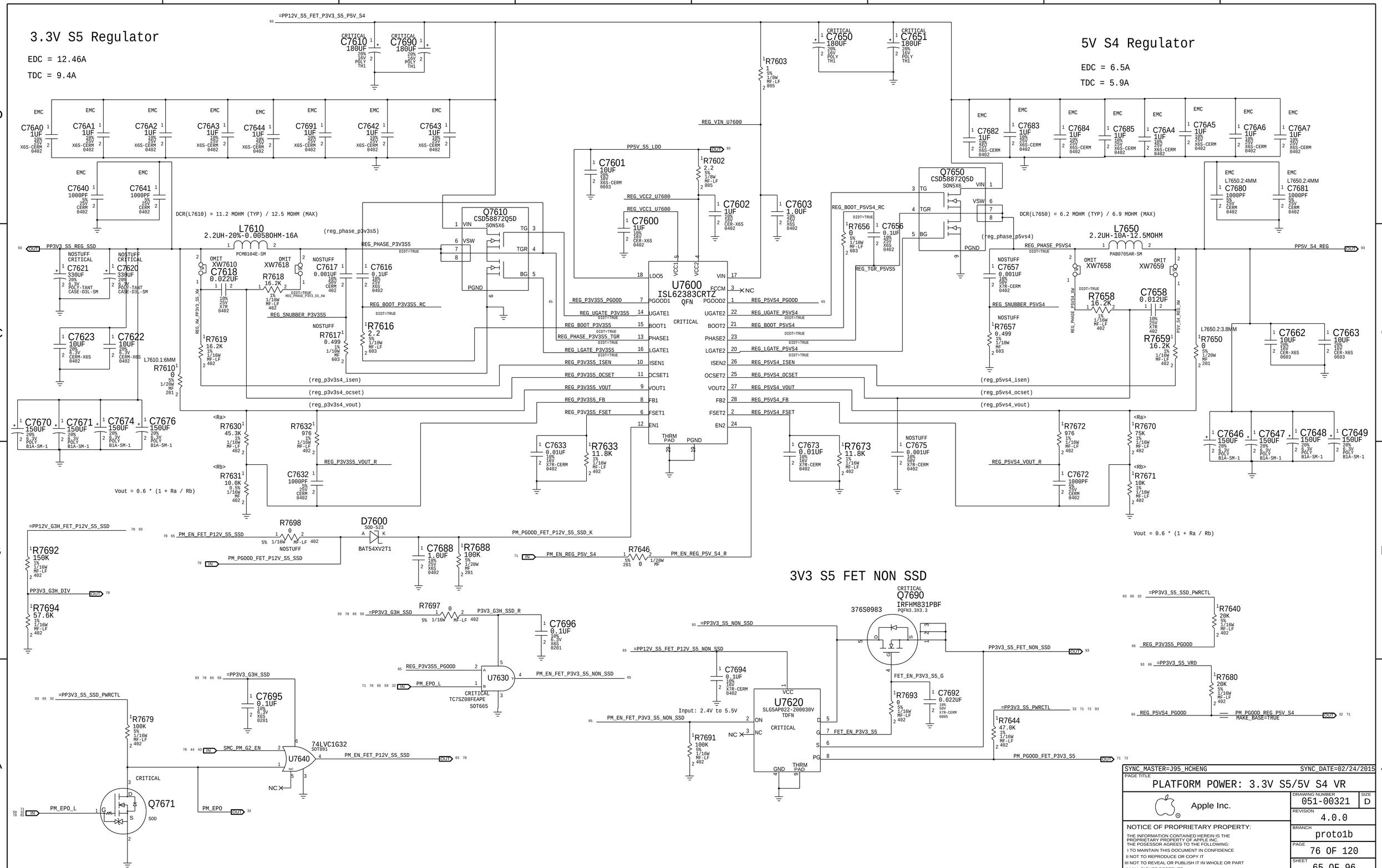
3.3V S5 Regulator
EDC = 12.46A
TDC = 9.4A
5V S4 Regulator
EDC = 6.5A
TDC = 5.9A
=PP12V_S5_FET_P3V3_S5_P5V_S4
PP5V_S5_LDO
REG_VIN_U7600
REG_VCC2_U7600
REG_VCC1_U7600
DCR(L7610) = 11.2 MOHM (TYP) / 12.5 MOHM (MAX)
DCR(L7650) = 6.2 MOHM (TYP) / 6.9 MOHM (MAX)
L7610
2.2UH-20%-0.00580HM-16A
L7650
2.2UH-10A-12.5MOHM
PP3V3_S5_REG_SSD
PP5V_S4_REG
U7600
ISL62383CRTZ
QFN
CRITICAL
Q7610
CSD58872Q5D
Q7650
CSD58872Q5D
Vout = 0.6 * (1 + Ra / Rb)
=PP12V_G3H_FET_P12V_S5_SSD
PM_EN_FET_P12V_S5_SSD
PM_PGOOD_FET_P12V_S5_SSD
PM_PGOOD_FET_P12V_S5_SSD_K
D7600
BAT54XV2T1
PM_EN_REG_P5V_S4
PM_EN_REG_P5V_S4_R
PP3V3_G3H_DIV
=PP3V3_G3H_SSD
P3V3_G3H_SSD_R
U7630
CRITICAL
TC7SZ08FEAPE
SOT665
PM_EPO_L
PM_EN_FET_P3V3_S5_NON_SSD
=PP3V3_S5_SSD_PWRCTL
Q7671
SOD
SMC_PM_G2_EN
U7640
74LVC1G32
SOT891
PM_EN_FET_P12V_S5_SSD
PM_EPO
=PP3V3_S5_NON_SSD
=PP12V_S5_FET_P12V_S5_NON_SSD
3V3 S5 FET NON SSD
Q7690
IRFHM831PBF
PQFN3.3X3.3
376S0983
PP3V3_S5_FET_NON_SSD
U7620
SLG5AP022-200030V
TDFN
Input: 2.4V to 5.5V
FET_EN_P3V3_S5_G
PM_PGOOD_FET_P3V3_S5
=PP3V3_S5_PWRCTL
=PP3V3_S5_SSD_PWRCTL
REG_P3V3S5_PGOOD
=PP3V3_S5_VRD
REG_P5VS4_PGOOD
PM_PGOOD_REG_P5V_S4
MAKE_BASE=TRUE
SYNC_MASTER=J95_HCHENG
SYNC_DATE=02/24/2015
PAGE TITLE
PLATFORM POWER: 3.3V S5/5V S4 VR
Apple Inc.
DRAWING NUMBER
051-00321
SIZE
D
REVISION
4.0.0
BRANCH
proto1b
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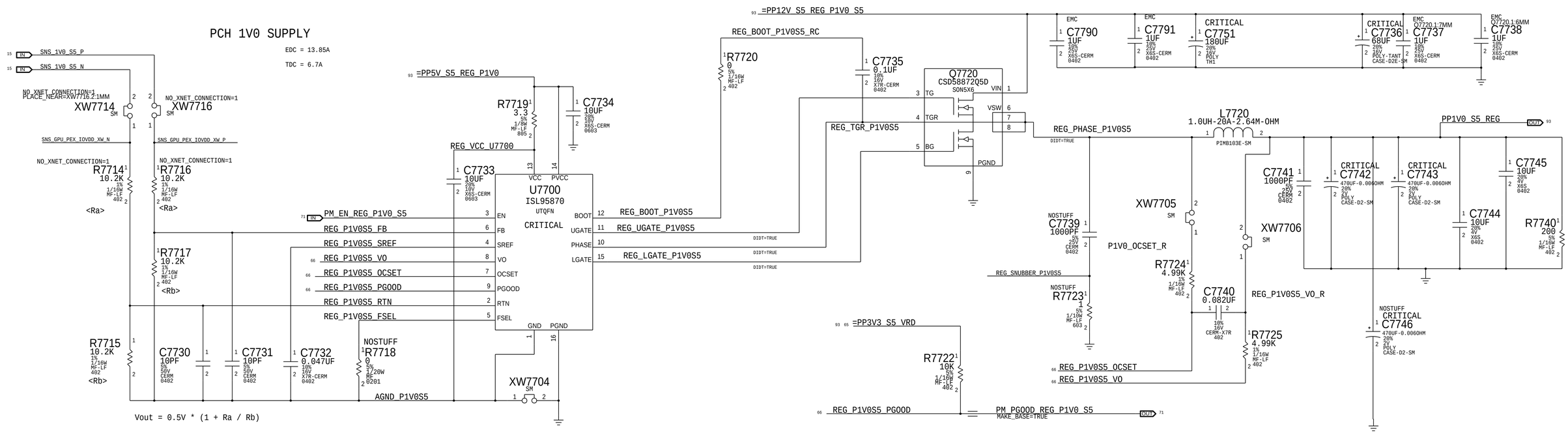

SYNC_MASTER=J95_HCHENG SYNC_DATE=02/24/2015

PAGE TITLE

CPU & CHIPSET: PCH 1V0 VR

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

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BRANCH proto1b

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SHEET 66 OF 96

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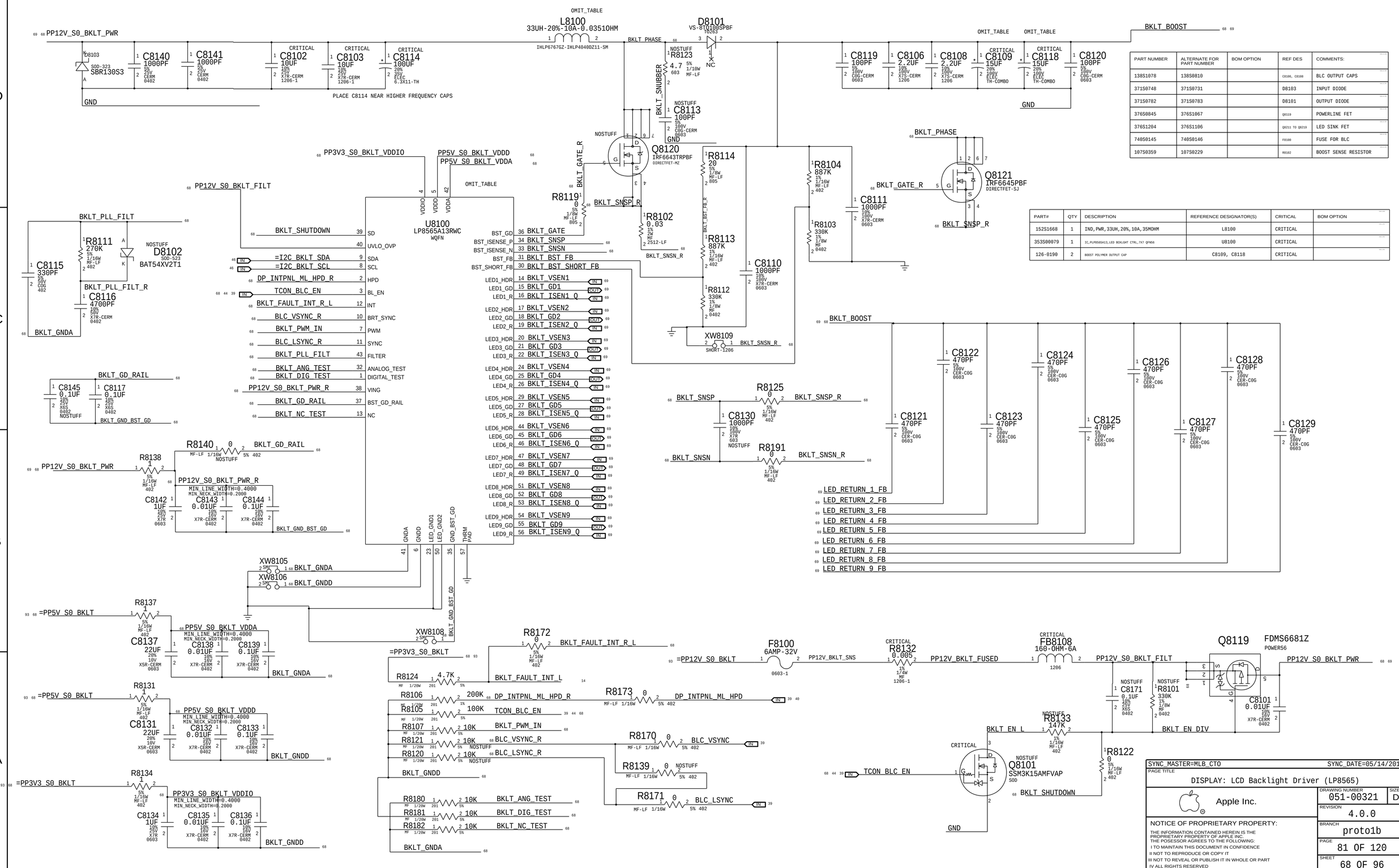
OMIT/table L8100 due to late sourcing change, did not want footprint change
Add 152s1668 (Cyntec) directly for next program



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S1078	138S0810		C8106, C8108	BLC OUTPUT CAPS
371S0748	371S0731		D8103	INPUT DIODE
371S0782	371S0783		D8101	OUTPUT DIODE
376S0845	376S1067		Q8119	POWERLINE FET
376S1204	376S1106		Q8211 TO Q8219	LED SINK FET
740S0145	740S0146		F8100	FUSE FOR BLC
107S0359	107S0229		R8102	BOOST SENSE RESISTOR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1668	1	IND,PWR,33UH,20%,10A,35MOHM	L8100	CRITICAL	
353S00079	1	IC,PLP8565A13,LED BCKLGHT CTRL,7X7 QFN56	U8100	CRITICAL	
126-0190	2	BOOST POLYMER OUTPUT CAP	C8109, C8118	CRITICAL	

SYNC_MASTER=MLB_CTO SYNC_DATE=05/14/2014

PAGE TITLE
DISPLAY: LCD Backlight Driver (LP8565)

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D
REVISION 4.0.0
BRANCH proto1b
PAGE 81 OF 120
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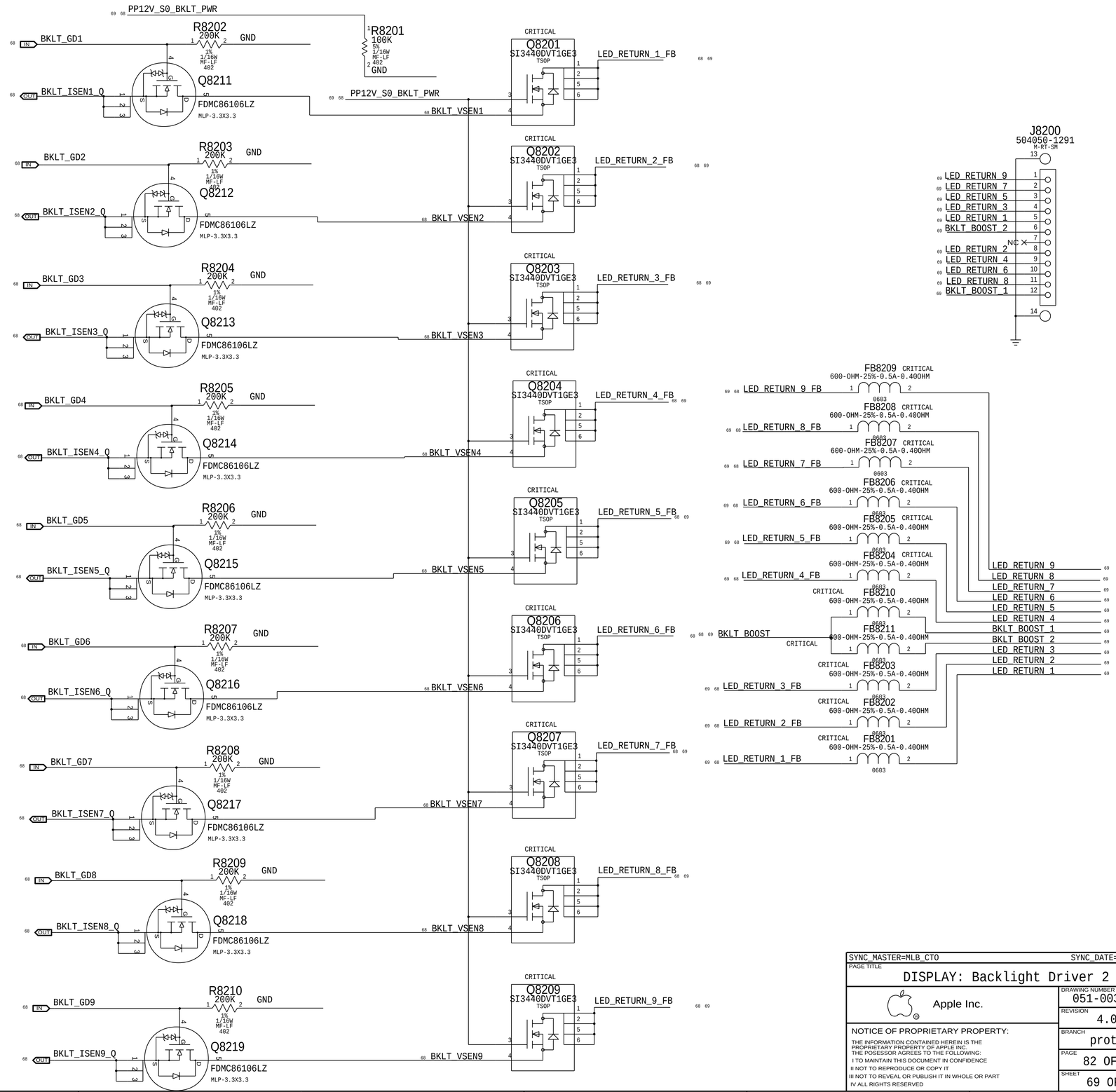
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1256	376S1073		ALL	Short Protection FET
155S0831	155S0797		ALL	FB8201 TO FB8211



SYNC_MASTER=MLB_CTO SYNC_DATE=05/14/2014

PAGE TITLE
DISPLAY: Backlight Driver 2

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D
REVISION 4.0.0
BRANCH proto1b
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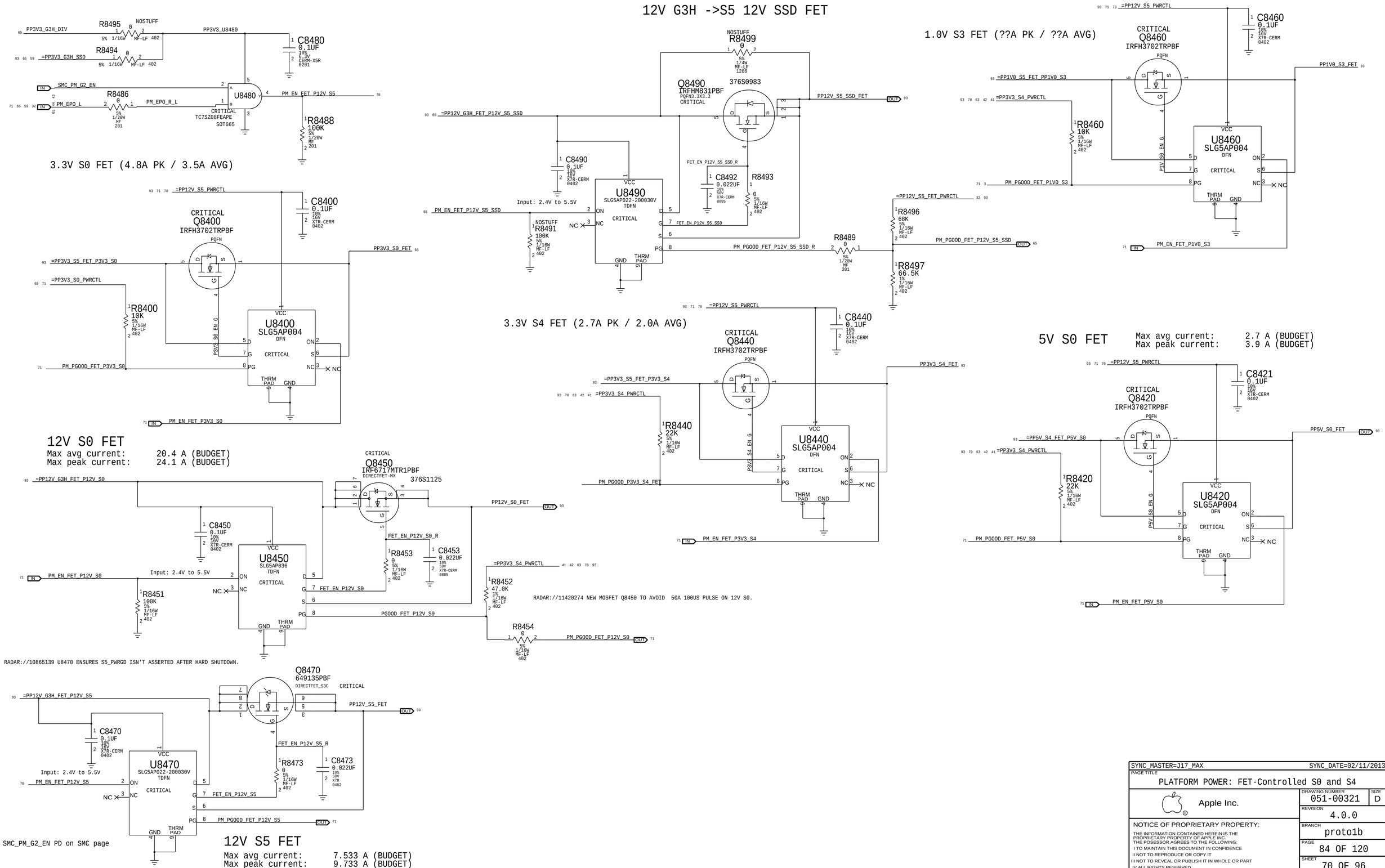

SYNC_MASTER=J17_MAX	SYNC_DATE=02/11/2013
PAGE TITLE	PLATFORM POWER: FET-Controlled S0 and S4
Apple Inc.	DRAWING NUMBER 051-00321 · SIZE D
	REVISION 4.0.0
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	PAGE 84 OF 120
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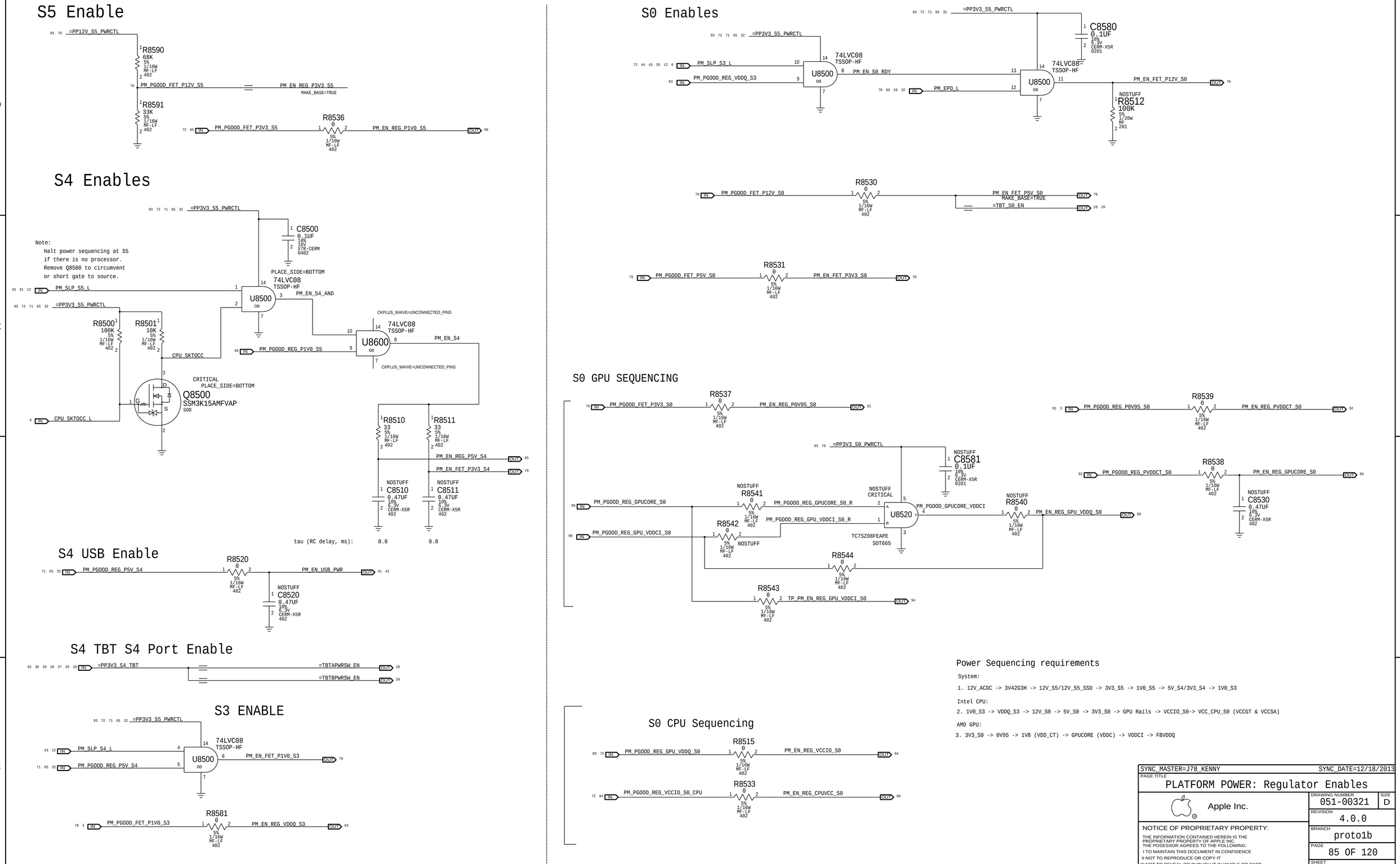
S5 Enable
=PP12V_S5_PWRCTL
R8590 68K 5% 1/16W MF-LF 402
PM_PGOOD_FET_P12V_S5
PM_EN_REG_P3V3_S5
MAKE_BASE=TRUE
R8591 33K 5% 1/16W MF-LF 402
PM_PGOOD_FET_P3V3_S5
R8536 0 5% 1/16W MF-LF 402
PM_EN_REG_P1V0_S5
S4 Enables
=PP3V3_S5_PWRCTL
C8500 0.1UF 10% 16V X7R-CERM 0402
Note:
Halt power sequencing at S5
if there is no processor.
Remove Q8500 to circumvent
or short gate to source.
PLACE_SIDE=BOTTOM
PM_SLP_S5_L
U8500 74LVC08 TSSOP-HF
PM_EN_S4_AND
R8500 100K 5% 1/16W MF-LF 402
R8501 10K 5% 1/16W MF-LF 402
CPU_SKTOCC
CKPLUS_WAIVE=UNCONNECTED_PINS
U8600 74LVC08 TSSOP-HF
PM_PGOOD_REG_P1V0_S5
PM_EN_S4
CRITICAL
PLACE_SIDE=BOTTOM
Q8500 SSM3K15AMFVAP SOD
CPU_SKTOCC_L
R8510 33 5% 1/16W MF-LF 402
R8511 33 5% 1/16W MF-LF 402
PM_EN_REG_P5V_S4
PM_EN_FET_P3V3_S4
NOSTUFF C8510 0.47UF 10% 6.3V CERM-X5R 402
NOSTUFF C8511 0.47UF 10% 6.3V CERM-X5R 402
tau (RC delay, ms): 0.0 0.0
S4 USB Enable
PM_PGOOD_REG_P5V_S4
R8520 0 5% 1/16W MF-LF 402
PM_EN_USB_PWR
NOSTUFF C8520 0.47UF 10% 6.3V CERM-X5R 402
S4 TBT S4 Port Enable
=PP3V3_S4_TBT
=TBTAPWRSW_EN
=TBTBPWRSW_EN
S3 ENABLE
=PP3V3_S5_PWRCTL
PM_SLP_S4_L
PM_PGOOD_REG_P5V_S4
U8500 74LVC08 TSSOP-HF
PM_EN_FET_P1V0_S3
R8581 0 5% 1/16W MF-LF 402
PM_PGOOD_FET_P1V0_S3
PM_EN_REG_VDDQ_S3
S0 Enables
=PP3V3_S5_PWRCTL
PM_SLP_S3_L
PM_PGOOD_REG_VDDQ_S3
U8500 74LVC08 TSSOP-HF
PM_EN_S0_RDY
C8580 0.1UF 10% 6.3V CERM-X5R 0201
PM_EPO_L
PM_EN_FET_P12V_S0
NOSTUFF R8512 100K 5% 1/20W MF 201
R8530 0 5% 1/16W MF-LF 402
PM_PGOOD_FET_P12V_S0
PM_EN_FET_P5V_S0
MAKE_BASE=TRUE
=TBT_S0_EN
R8531 0 5% 1/16W MF-LF 402
PM_PGOOD_FET_P5V_S0
PM_EN_FET_P3V3_S0
S0 GPU SEQUENCING
R8537 0 5% 1/16W MF-LF 402
PM_PGOOD_FET_P3V3_S0
PM_EN_REG_P0V95_S0
R8539 0 5% 1/16W MF-LF 402
PM_PGOOD_REG_P0V95_S0
PM_EN_REG_PVDDCT_S0
=PP3V3_S0_PWRCTL
NOSTUFF C8581 0.1UF 10% 6.3V CERM-X5R 0201
R8538 0 5% 1/16W MF-LF 402
PM_PGOOD_REG_PVDDCT_S0
PM_EN_REG_GPUCORE_S0
NOSTUFF C8530 0.47UF 10% 6.3V CERM-X5R 402
PM_PGOOD_REG_GPUCORE_S0
NOSTUFF R8541 0 5% 1/16W MF-LF 402
PM_PGOOD_REG_GPUCORE_S0_R
NOSTUFF CRITICAL U8520 TC7SZ08FEAPE SOT665
PM_PGOOD_GPUCORE_VDDCI
NOSTUFF R8540 0 5% 1/16W MF-LF 402
PM_EN_REG_GPU_VDDQ_S0
PM_PGOOD_REG_GPU_VDDCI_S0
PM_PGOOD_REG_GPU_VDDCI_S0_R
NOSTUFF R8542 0 5% 1/16W MF-LF 402
R8544 0 5% 1/16W MF-LF 402
R8543 0 5% 1/16W MF-LF 402
TP_PM_EN_REG_GPU_VDDCI_S0
S0 CPU Sequencing
PM_PGOOD_REG_GPU_VDDQ_S0
R8515 0 5% 1/16W MF-LF 402
PM_EN_REG_VCCIO_S0
PM_PGOOD_REG_VCCIO_S0_CPU
R8533 0 5% 1/16W MF-LF 402
PM_EN_REG_CPUVCC_S0
Power Sequencing requirements
System:
1. 12V_ACDC -> 3V42G3H -> 12V_S5/12V_S5_SSD -> 3V3_S5 -> 1V0_S5 -> 5V_S4/3V3_S4 -> 1V0_S3
Intel CPU:
2. 1V0_S3 -> VDDQ_S3 -> 12V_S0 -> 5V_S0 -> 3V3_S0 -> GPU Rails -> VCCIO_S0-> VCC_CPU_S0 (VCCGT & VCCSA)
AMD GPU:
3. 3V3_S0 -> 0V95 -> 1V8 (VDD_CT) -> GPUCORE (VDDC) -> VDDCI -> FBVDDQ
SYNC_MASTER=J78_KENNY
SYNC_DATE=12/18/2013
PAGE TITLE
PLATFORM POWER: Regulator Enables
Apple Inc.
DRAWING NUMBER 051-00321
SIZE D
REVISION 4.0.0
BRANCH proto1b
PAGE 85 OF 120
SHEET 71 OF 96
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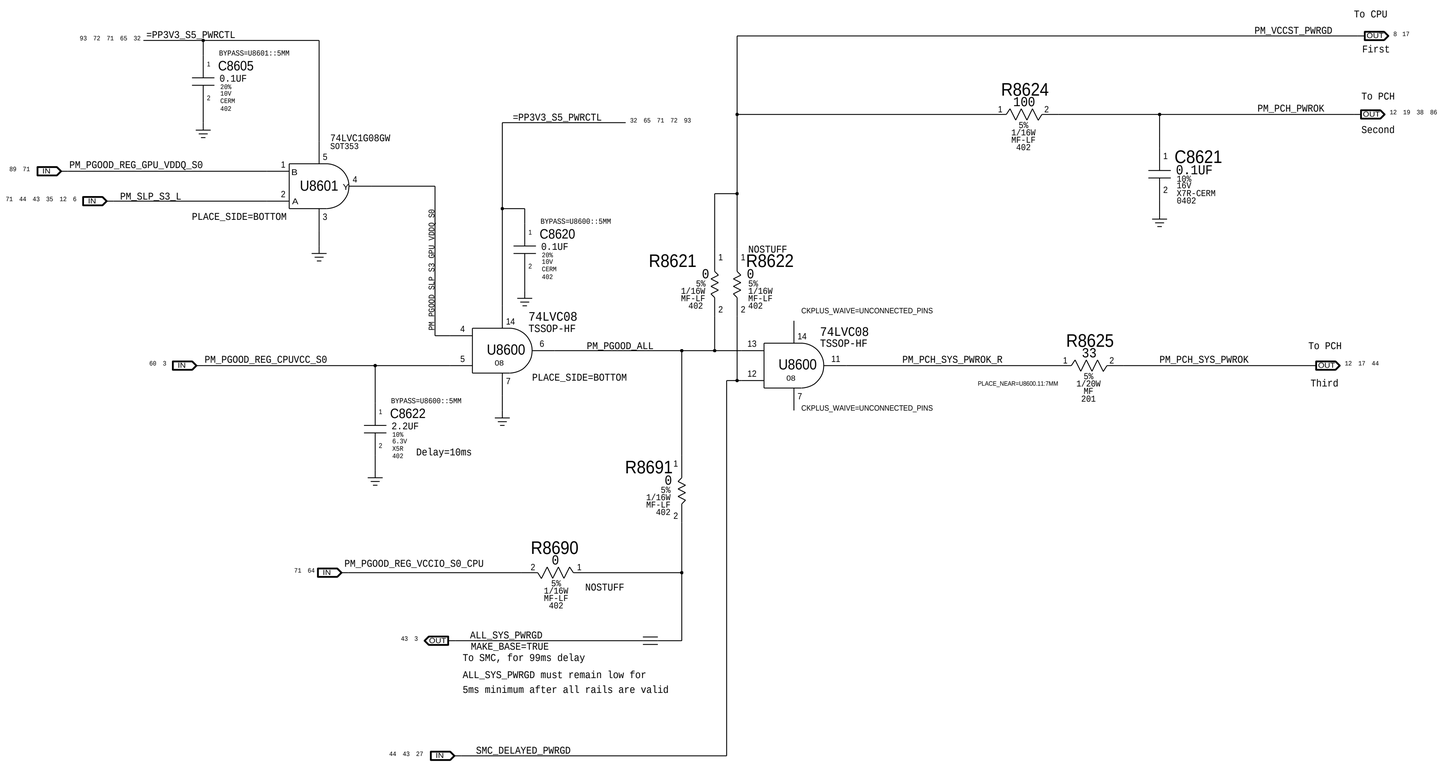
ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation

PCH Power Goods



Resume Reset

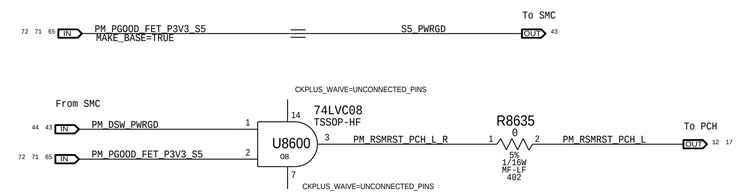
Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

Note:
THE IMAC J78 DESIGNS DOES NOT SUPPORT DEEP SX MODES SO BOTH DPWROK AND RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V
to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



SYNC_MASTER=J78_KENNY SYNC_DATE=10/09/2013

PAGE TITLE
PLATFORM POWER: PM Power Good

Apple Inc.

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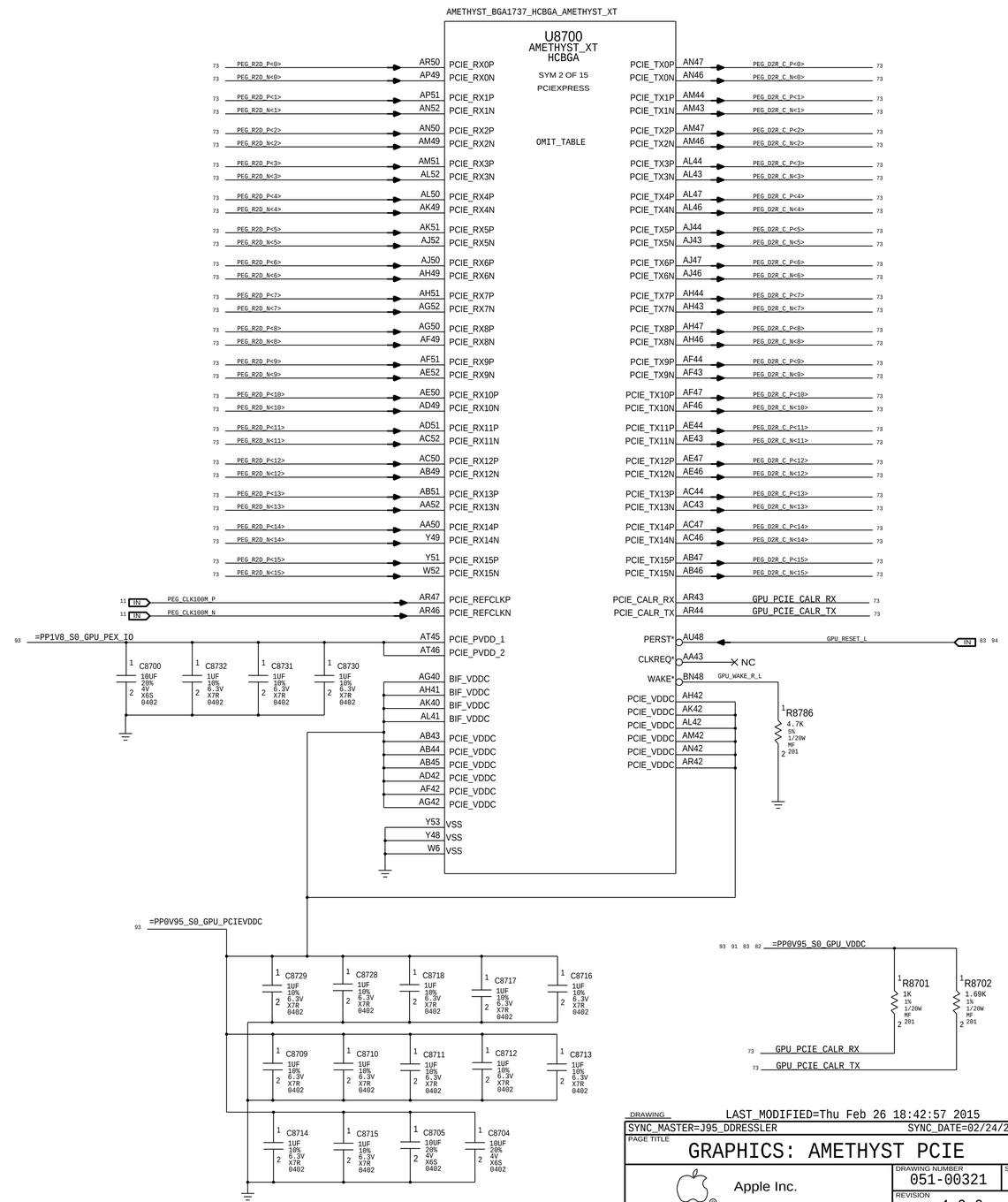
POLARITY SWAPS INTENDED ON LANES,SEE NOTES AT DIFF PAIRS.
ALL LANES ARE ALSO REVERSED, SEE ALIASES ON CSA 102

NOTE:
TONGA DOES NOT GENERATE PCIE CLKREQ.



DRAWING LAST_MODIFIED=Thu Feb 26 18:42:57 2015
SYNC_MASTER=J95_DDRESSLER SYNC_DATE=02/24/2015

PAGE TITLE
GRAPHICS: AMETHYST PCIE

Apple Inc.

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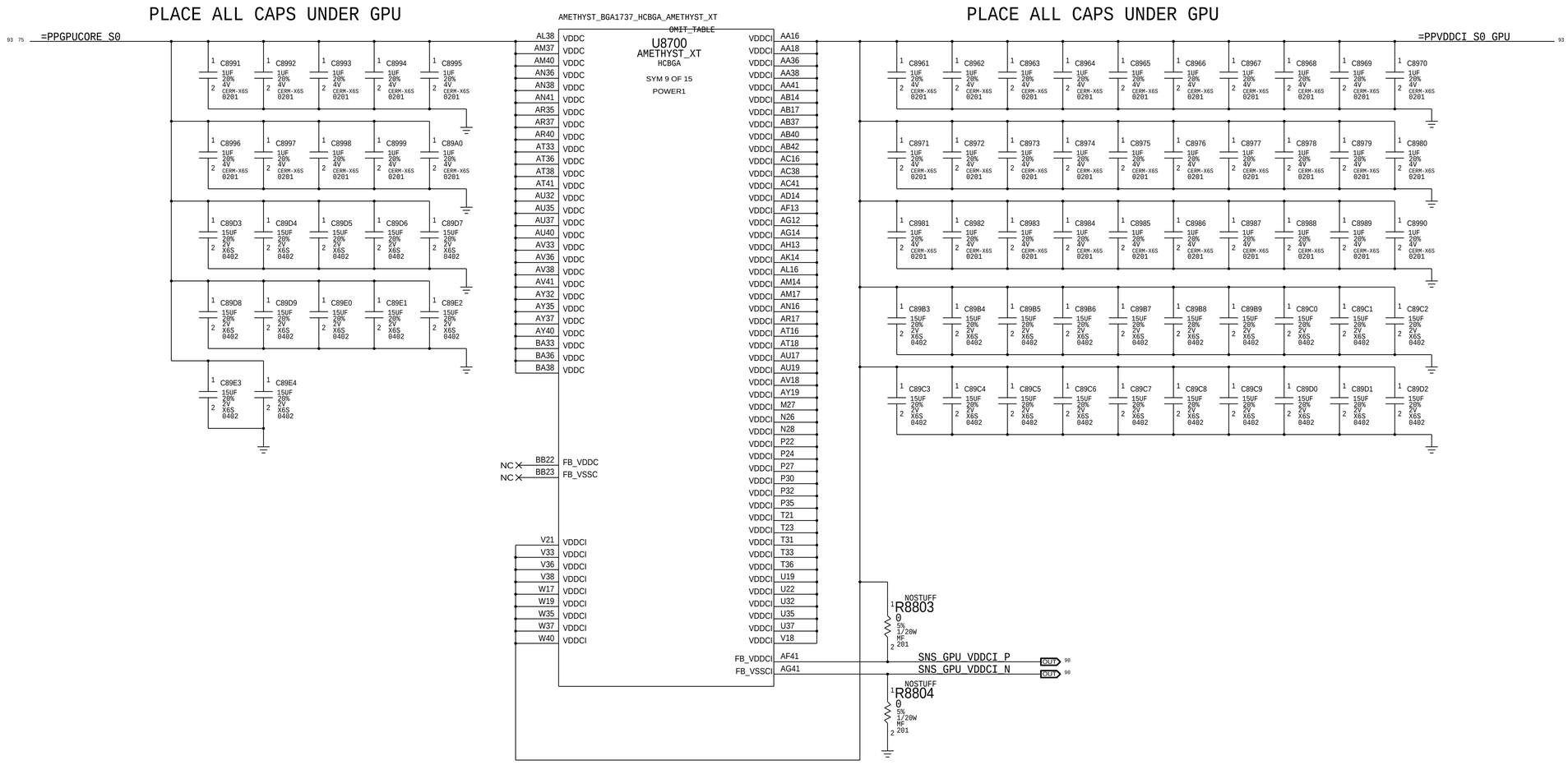
GPU VDDC/VDDCI DECOUPLING



DRAWING LAST_MODIFIED=Thu Feb 26 18:42:57 2015

SYNC_MASTER=J78_NAT SYNC_DATE=12/09/2013

PAGE TITLE

GRAPHICS: VDDC/VDDCI DECOUPLING

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REVISION 4.0.0

BRANCH proto1b

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GPU MVDD/VDDGFX DECOUPLING

=PPGPUCORE_S0 74 93

C8801 C8802 C8803 C8804 C8805 C8806 C8807 C8808 C8809 C8810
C8811 C8812 C8813 C8814 C8815 C8816 C8817 C8818 C8819 C8820
C8821 C8822 C8823 C8824 C8825 C8826 C8827 C8828 C8829 C8830
C8831 C8832 C8833 C8834 C8835 C8836 C8837 C8838 C8839 C8840
1UF 20% 4V CERM-X6S 0201

PLACE ALL CAPS UNDER GPU

C8863 C8864 C8865 C8866 C8867 C8868 C8869 C8870 C8871 C8872
15UF 20% 2V X6S 0402

C8873 C8874 C8875 C8876 C8877 C8878 C8879 C8880 C8881 C8882
15UF 20% 2V X6S 0402

C8883 C8884 C8885 C8886 C8887 C8888 C8889 C8890 C8891 C8892
15UF 20% 2V X6S 0402

C8893 C8894 C8895 C8896 C8897 C8898 C8899 C88A0 C88A1 C88A2
15UF 20% 2V X6S 0402

AMETHYST_BGA1737_HCBGA_AMETHYST_XT
OMIT_TABLE

U8700
AMETHYST_XT
HCBGA
SYM 10 OF 15
POWER 2

AA21	VDDGFX	VDDGFX	AL31
AA23	VDDGFX	VDDGFX	AL33
AA26	VDDGFX	VDDGFX	AL36
AA28	VDDGFX	VDDGFX	AM22
AA31	VDDGFX	VDDGFX	AM24
AA33	VDDGFX	VDDGFX	AM27
AB19	VDDGFX	VDDGFX	AM30
AB22	VDDGFX	VDDGFX	AM32
AB24	VDDGFX	VDDGFX	AM35
AB27	VDDGFX	VDDGFX	AN21
AB30	VDDGFX	VDDGFX	AN23
AB32	VDDGFX	VDDGFX	AN26
AB35	VDDGFX	VDDGFX	AN28
AC18	VDDGFX	VDDGFX	AN31
AC21	VDDGFX	VDDGFX	AN33
AC23	VDDGFX	VDDGFX	AR22
AC26	VDDGFX	VDDGFX	AR24
AC28	VDDGFX	VDDGFX	AR27
AC31	VDDGFX	VDDGFX	AR30
AC33	VDDGFX	VDDGFX	AR32
AC36	VDDGFX	VDDGFX	AT21
AD17	VDDGFX	VDDGFX	AT23
AD19	VDDGFX	VDDGFX	AT26
AD22	VDDGFX	VDDGFX	AT28
AD24	VDDGFX	VDDGFX	AT31
AD27	VDDGFX	VDDGFX	AU22
AD30	VDDGFX	VDDGFX	AU24
AD32	VDDGFX	VDDGFX	AU27
AD35	VDDGFX	VDDGFX	AU30
AD37	VDDGFX	VDDGFX	AV21
AD40	VDDGFX	VDDGFX	AV23
AF16	VDDGFX	VDDGFX	AV26
AF18	VDDGFX	VDDGFX	AV28
AF21	VDDGFX	VDDGFX	AV31
AF23	VDDGFX	VDDGFX	AY22
AF26	VDDGFX	VDDGFX	AY24
AF28	VDDGFX	VDDGFX	AY27
AF31	VDDGFX	VDDGFX	AY30
AF33	VDDGFX	VDDGFX	BA21
AF36	VDDGFX	VDDGFX	BA23
AF38	VDDGFX	VDDGFX	BA26
AG17	VDDGFX	VDDGFX	BA28
AG19	VDDGFX	VDDGFX	BA31
AG22	VDDGFX	VDDGFX	BB24
AG24	VDDGFX	VDDGFX	BB27
AG27	VDDGFX	VDDGFX	BB30
AG30	VDDGFX	VDDGFX	BB32
AG32	VDDGFX	VDDGFX	T26
AG35	VDDGFX	VDDGFX	T28
AG37	VDDGFX	VDDGFX	U24
AH16	VDDGFX	VDDGFX	U27
AH18	VDDGFX	VDDGFX	U30
AH21	VDDGFX	VDDGFX	V23
AH23	VDDGFX	VDDGFX	V26
AH26	VDDGFX	VDDGFX	V28
AH28	VDDGFX	VDDGFX	V31
AH31	VDDGFX	VDDGFX	W22
AH33	VDDGFX	VDDGFX	W24
AH36	VDDGFX	VDDGFX	W27
AH38	VDDGFX	VDDGFX	W30
AK17	VDDGFX	VDDGFX	W32
AK19	VDDGFX		
AK22	VDDGFX		
AK24	VDDGFX		
AK27	VDDGFX		
AK30	VDDGFX		
AK32	VDDGFX		
AK35	VDDGFX		
AK37	VDDGFX		
AL18	VDDGFX		
AL21	VDDGFX		
AL23	VDDGFX		
AL26	VDDGFX		
AL28	VDDGFX		

NOSTUFF
R8901
0 5% 1/20W MF 201

FB_VSSGFX BB33 VSNS_GPU_VSS OUT 86
FB_VDDGFX BB31 VSNS_GPU_VDD OUT 86

NOSTUFF
R8902
0 5% 1/20W MF 201

=PP1V35_S0_GPU_FBVDDQ 76 77 78 79 80 81 89 93

PLACE ALL CAPS UNDER GPU

C8901 C8902 C8903 C8904 C8905 C8906 C8907 C8908 C8909 C8910
C8911 C8912 C8913 C8914 C8915 C8916 C8917 C8918 C8919 C8920
C8921 C8922 C8923 C8924 C8925 C8926 C8927 C8928 C8929 C8930
C8931 C8932 C8933 C8934 C8935 C8936 C8937 C8938 C8939 C8940
C8941 C8942 C8943 C8944 C8945 C8946 C8955 C8956 C8957 C8958
1UF 20% 4V CERM-X6S 0201

AMETHYST_BGA1737_HCBGA_AMETHYST_XT
OMIT_TABLE

U8700
AMETHYST_XT
HCBGA
SYM 11 OF 15

AA13	VMEMIO	RSVD	AM18
AA6	VMEMIO	RSVD	AM19
AB12	VMEMIO	RSVD	AN18
AC13	VMEMIO	RSVD	AN19
AE6	VMEMIO	RSVD	AR18
AJ6	VMEMIO	RSVD	AR19
AL13	VMEMIO	RSVD	AR48
AM12	VMEMIO	RSVD	AT42
AN13	VMEMIO	RSVD	AT43
AN6	VMEMIO	RSVD	AT44
AR14	VMEMIO	RSVD	AT47
AT13	VMEMIO	RSVD	AT48
AU14	VMEMIO	RSVD	AU42
AU6	VMEMIO	RSVD	AV51
AV13	VMEMIO	RSVD	AV53
AV16	VMEMIO	RSVD	AY41
AY14	VMEMIO	RSVD	AY44
AY17	VMEMIO	RSVD	BA41
BA18	VMEMIO	RSVD	BC43
BA6	VMEMIO	RSVD	BC52
BB19	VMEMIO	RSVD	BD40
BC11	VMEMIO	RSVD	BD51
BE6	VMEMIO	RSVD	BF45
BE9	VMEMIO	RSVD	BF47
BF8	VMEMIO	RSVD	BF48
BG7	VMEMIO	RSVD	BG42
BH13	VMEMIO	RSVD	BG43
BH9	VMEMIO	RSVD	BG45
F13	VMEMIO	RSVD	BG47
F17	VMEMIO	RSVD	BG48
F21	VMEMIO	RSVD	BH42
F25	VMEMIO	RSVD	BH43
F29	VMEMIO	RSVD	BH44
F33	VMEMIO	RSVD	BH45
F37	VMEMIO	RSVD	BJ42
F41	VMEMIO	RSVD	BL18
F45	VMEMIO	RSVD	BL49
F9	VMEMIO	RSVD	BN18
G47	VMEMIO	RSVD	T48
G7	VMEMIO	RSVD	T49
H46	VMEMIO	RSVD	U48
J45	VMEMIO	RSVD	V51
J48	VMEMIO		
J6	VMEMIO		
L43	VMEMIO		
M14	VMEMIO		
M22	VMEMIO		
M32	VMEMIO		
N13	VMEMIO		
N16	VMEMIO		
N18	VMEMIO		
N21	VMEMIO		
N23	VMEMIO		
N31	VMEMIO		
N33	VMEMIO		
N36	VMEMIO		
N38	VMEMIO		
N48	VMEMIO		
N6	VMEMIO		
P12	VMEMIO		
P14	VMEMIO		
P17	VMEMIO		
P19	VMEMIO		
P37	VMEMIO		
P40	VMEMIO		
T13	VMEMIO		
T18	VMEMIO		
T38	VMEMIO		
U14	VMEMIO		
U17	VMEMIO		
U40	VMEMIO		
U6	VMEMIO		
V13	VMEMIO		
V16	VMEMIO		
V41	VMEMIO		
W14	VMEMIO		
W42	VMEMIO		

DRAWING LAST_MODIFIED=Thu Feb 26 18:42:58 2015
SYNC_MASTER=J78_NAT SYNC_DATE=12/09/2013
PAGE TITLE
GRAPHICS: MVDD/VDDGFX DECOUPLING

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D
REVISION 4.0.0
BRANCH proto1b
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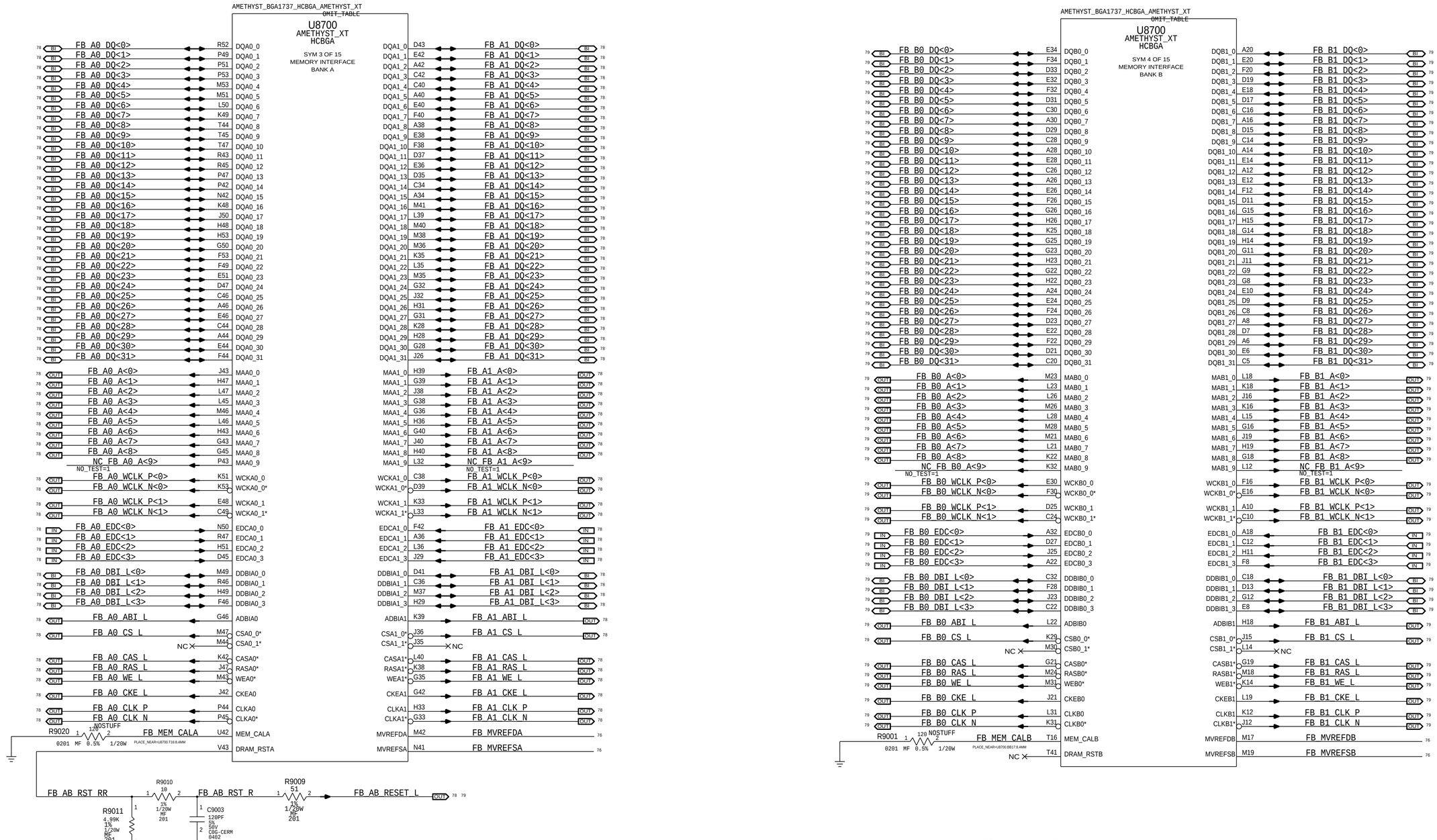

DRAWING LAST_MODIFIED=Thu Feb 26 18:42:58 2015

SYNC_MASTER=J78_PETER SYNC_DATE=12/04/2013

PAGE TITLE

GRAPHICS: FRAME BUFFER A/B

Apple Inc.

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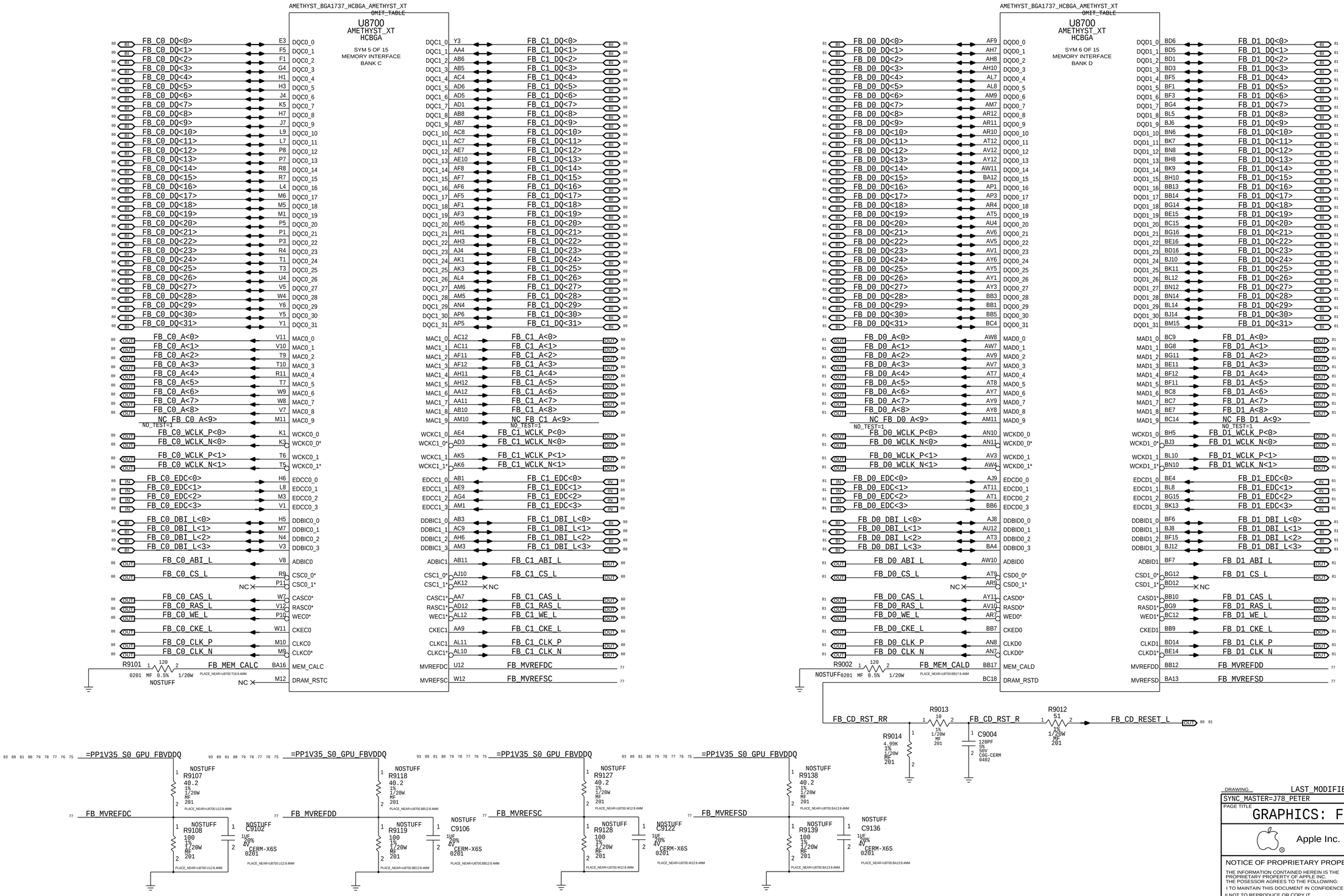

DRAWING LAST_MODIFIED=Thu Feb 26 18:42:58 2015

SYNC_MASTER=J78_PETER SYNC_DATE=12/04/2013

PAGE TITLE

GRAPHICS: FRAME BUFFER C/D

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

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Page Notes

Power aliases required by this page:

- =PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

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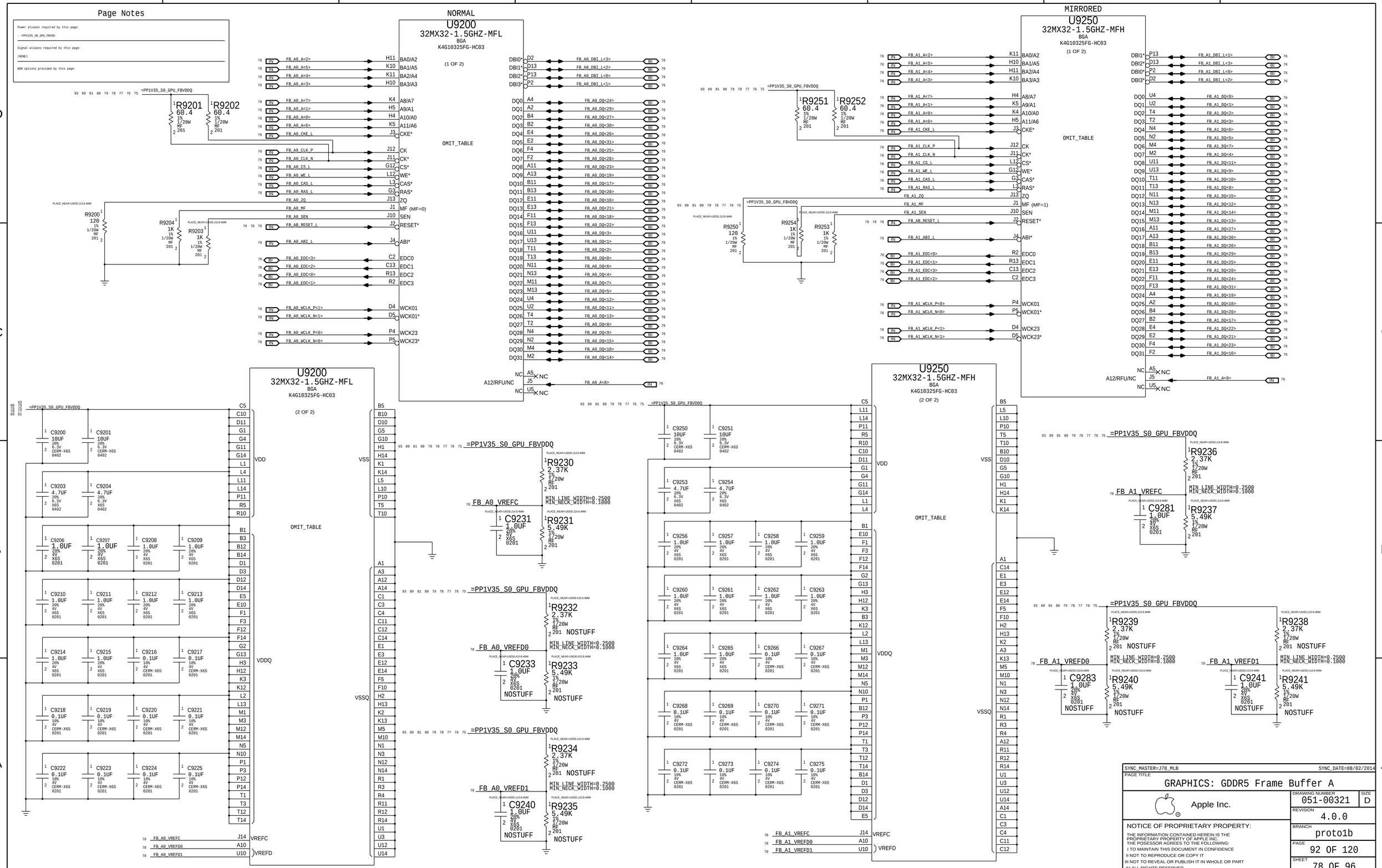

SYNC_MASTER=J78_MLB	SYNC_DATE=08/02/2014
PAGE TITLE	GRAPHICS: GDDR5 Frame Buffer A
Apple Inc.	DRAWING NUMBER 051-00321 · SIZE D
	REVISION 4.0.0
	BRANCH proto1b
	PAGE 92 OF 120
	SHEET 78 OF 96

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- =PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

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BOM options provided by this page:

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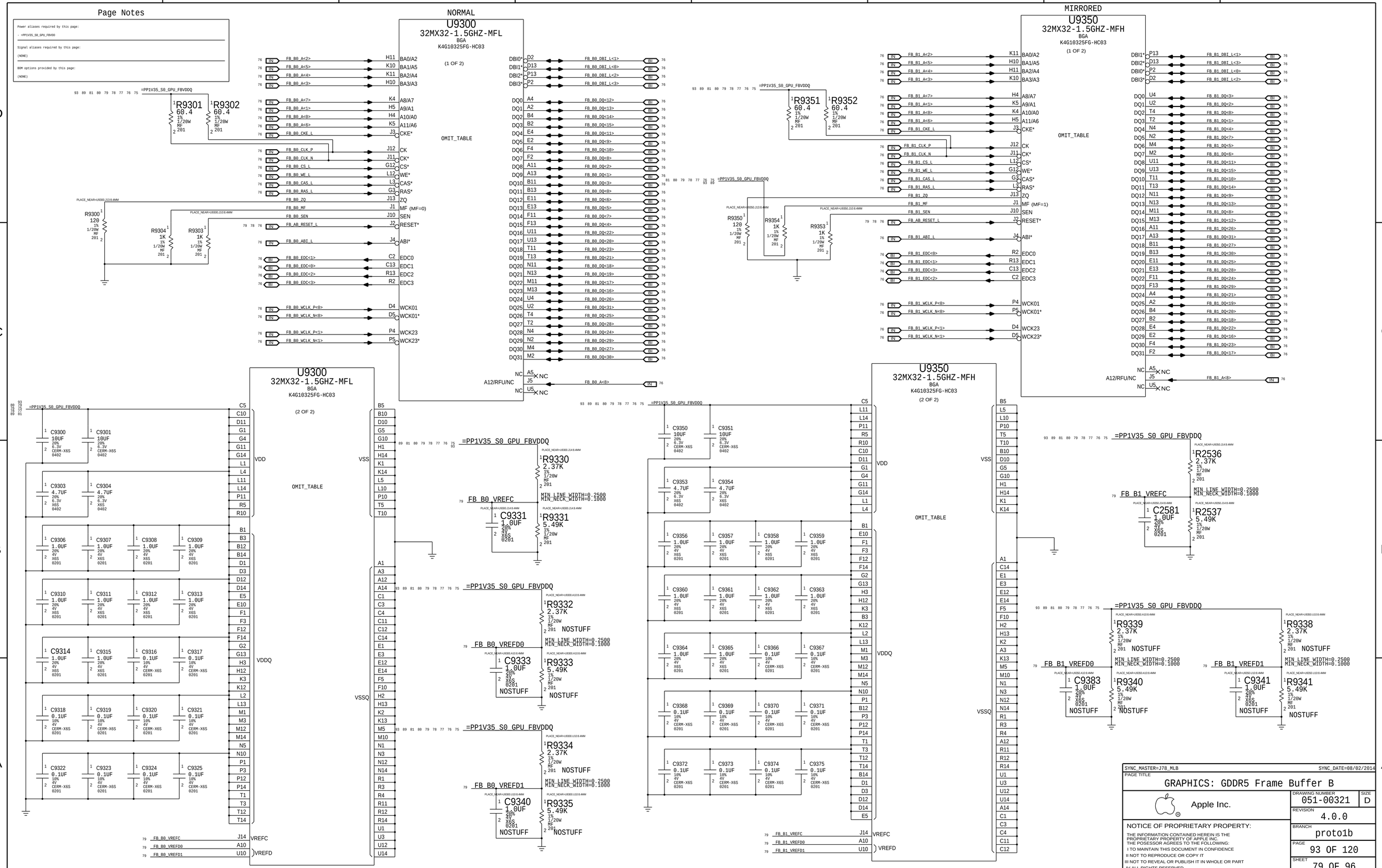

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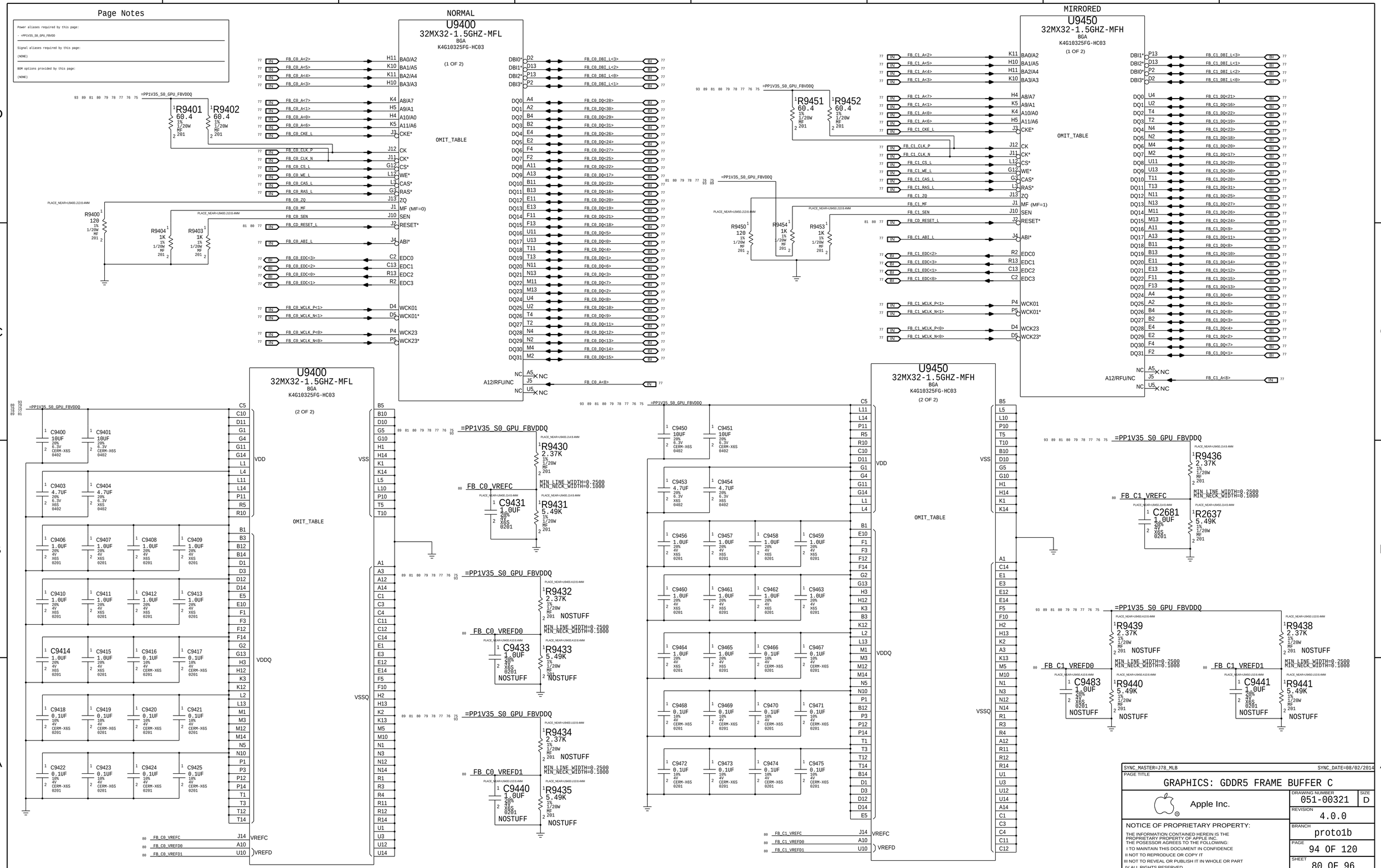

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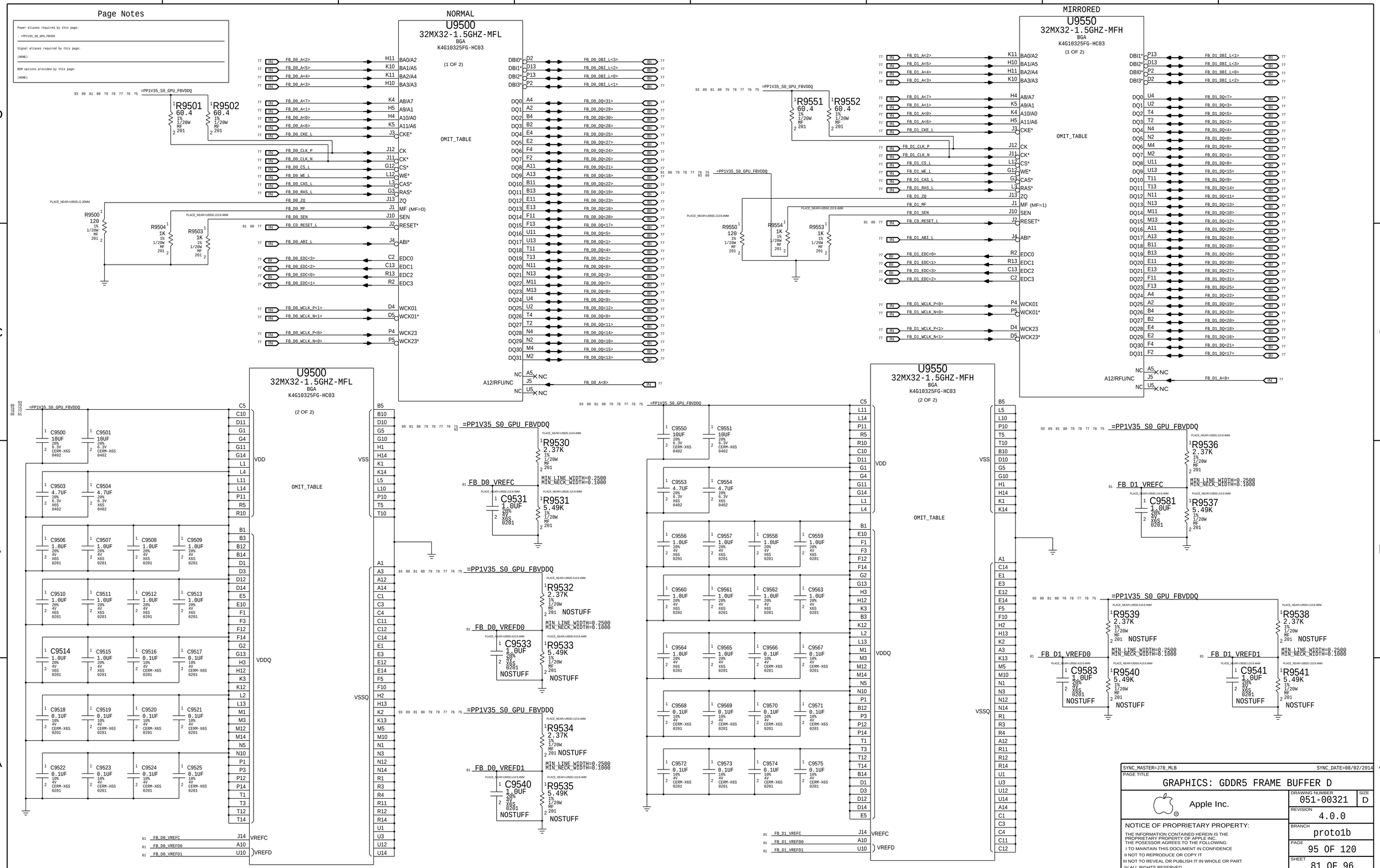

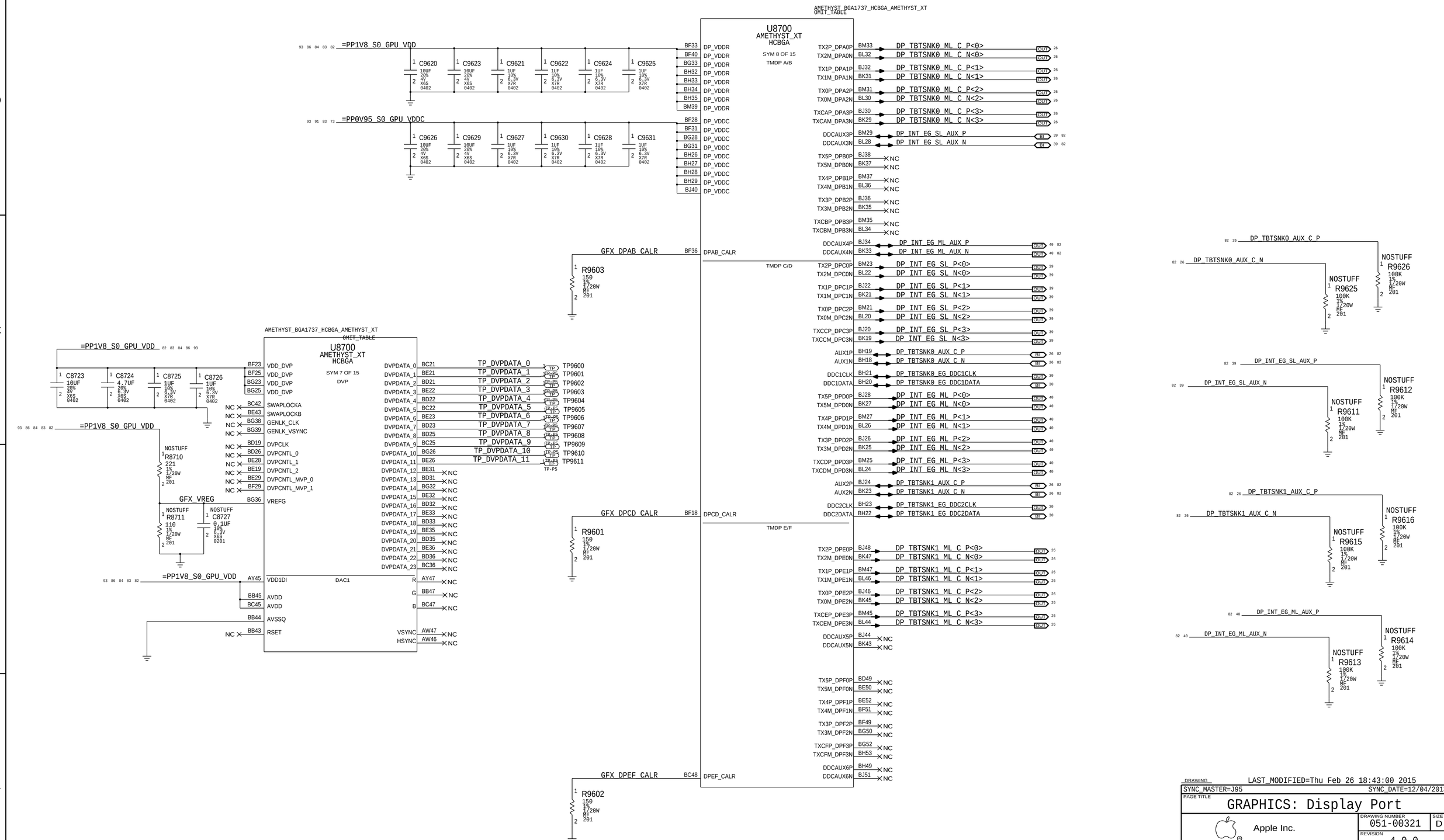

DRAWING LAST_MODIFIED=Thu Feb 26 18:43:00 2015

SYNC_MASTER=J95 SYNC_DATE=12/04/2013

PAGE TITLE

GRAPHICS: Display Port

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

PAGE 96 OF 120

SHEET 82 OF 96

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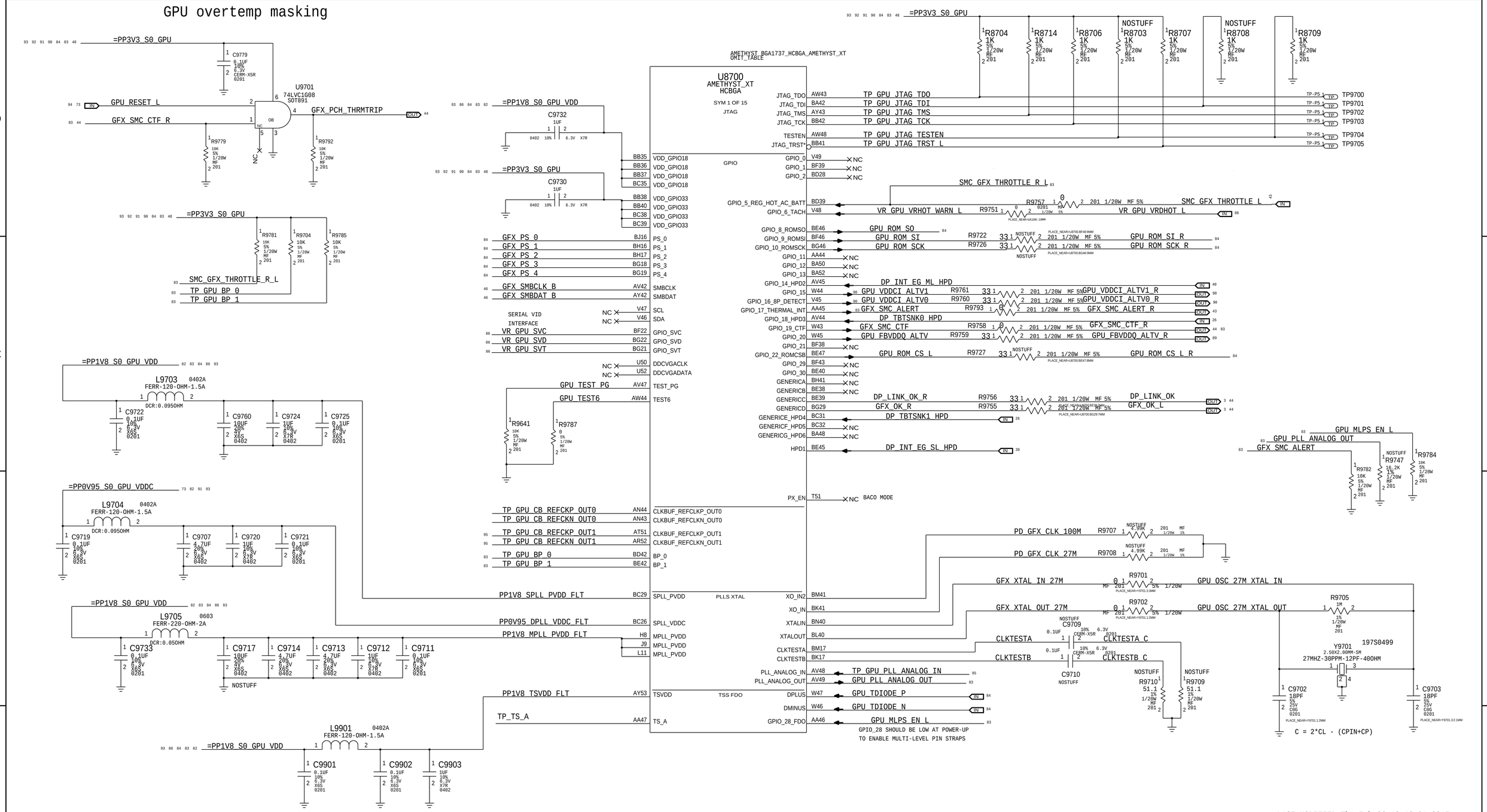
GPU overtemp masking



DRAWING LAST_MODIFIED=Thu Feb 26 18:43:01 2015

SYNC_MASTER=J95_DDRESSLER SYNC_DATE=02/24/2015

PAGE TITLE

GRAPHICS: GPU GPIOS/PLLS/STRAPS

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

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BRANCH proto1b

PAGE 97 OF 120

SHEET 83 OF 96

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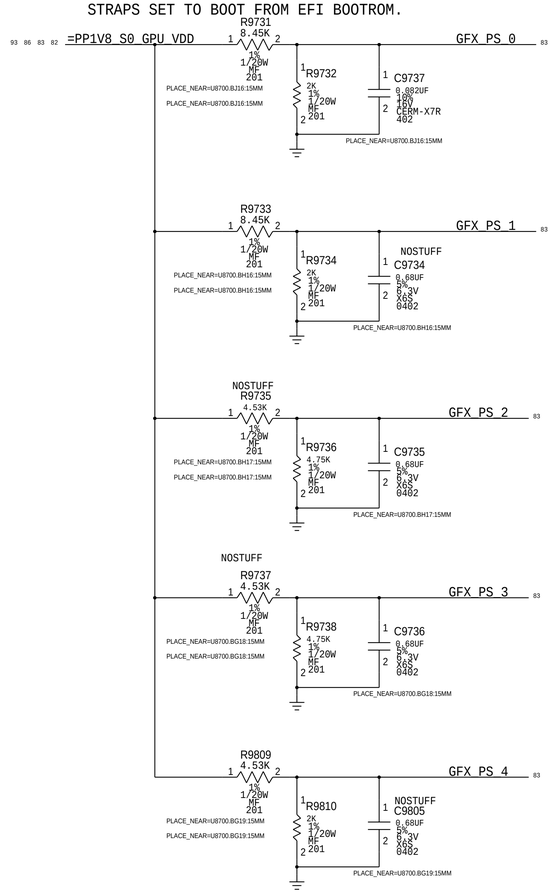
CONFIG STRAPS - MLS

STRAPS SET TO BOOT FROM EFI BOOTROM.



SMC KEY

	GFXA
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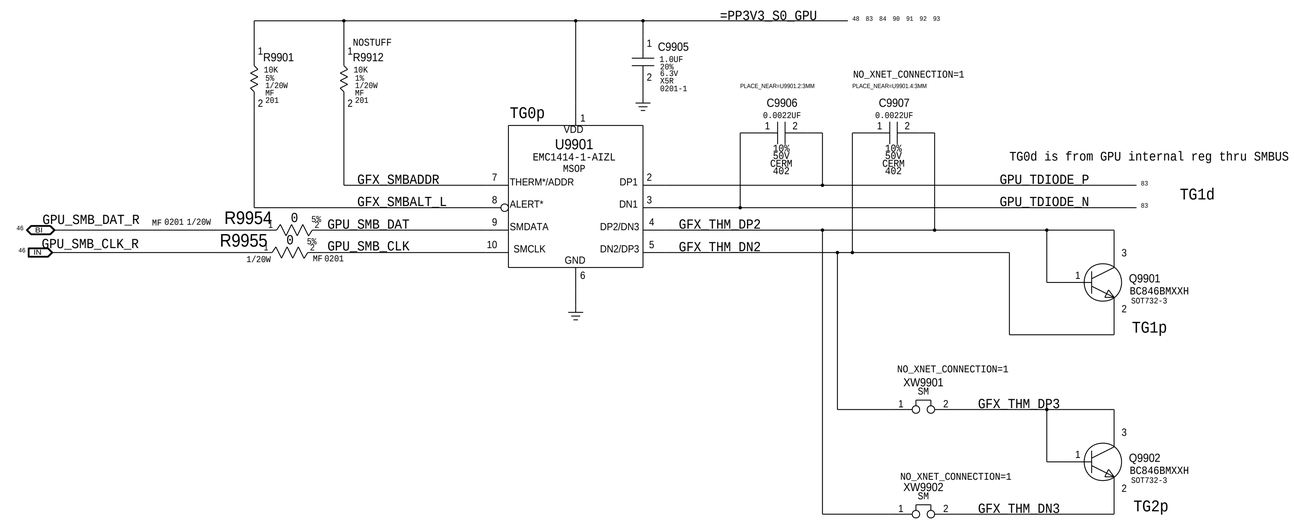
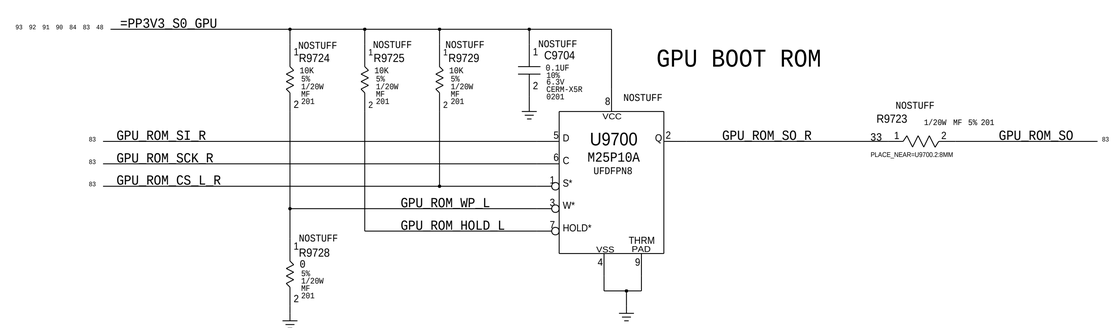
GPU VRAM Prox Temp	TG1p
GPU VR Prox Temp	TG2p
GPU TDiode Temp	TG1d





Page Notes

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- +PP3V3_S0_GPU
- +PP1V8_S0_GPU_MIX_PLL400

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

SYNC_MASTER=J78_PETER	SYNC_DATE=11/13/2013
PAGE TITLE	GRAPHICS: GPU STRAPS,SENSORS,ROM
Apple Inc.	DRAWING NUMBER 051-00321 SIZE D
	REVISION 4.0.0
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	PAGE 98 OF 120
	SHEET 84 OF 96

AMETHYST_BGA1737_HCBGA_AMETHYST_XT
OMIT_TABLE

U8700
AMETHYST_XT
HCBGA
SYM 12 OF 15
GND 1

A4	VSS	VSS	AF40
A48	VSS	VSS	AF45
A50	VSS	VSS	AF48
AA10	VSS	VSS	AF53
AA14	VSS	VSS	AG13
AA17	VSS	VSS	AG16
AA19	VSS	VSS	AG18
AA2	VSS	VSS	AG2
AA22	VSS	VSS	AG21
AA24	VSS	VSS	AG23
AA27	VSS	VSS	AG26
AA30	VSS	VSS	AG28
AA32	VSS	VSS	AG31
AA35	VSS	VSS	AG33
AA37	VSS	VSS	AG36
AA40	VSS	VSS	AG38
AA42	VSS	VSS	AG48
AA48	VSS	VSS	AG6
AA8	VSS	VSS	AH14
AB13	VSS	VSS	AH17
AB16	VSS	VSS	AH19
AB18	VSS	VSS	AH22
AB21	VSS	VSS	AH24
AB23	VSS	VSS	AH27
AB26	VSS	VSS	AH30
AB28	VSS	VSS	AH32
AB31	VSS	VSS	AH35
AB33	VSS	VSS	AH37
AB36	VSS	VSS	AH40
AB38	VSS	VSS	AH45
AB41	VSS	VSS	AH48
AB48	VSS	VSS	AH53
AB53	VSS	VSS	AH9
AB9	VSS	VSS	AJ11
AC10	VSS	VSS	AJ2
AC14	VSS	VSS	AJ45
AC17	VSS	VSS	AJ48
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AC27	VSS	VSS	AK21
AC30	VSS	VSS	AK23
AC32	VSS	VSS	AK26
AC35	VSS	VSS	AK28
AC37	VSS	VSS	AK31
AC40	VSS	VSS	AK33
AC42	VSS	VSS	AK36
AC45	VSS	VSS	AK38
AC48	VSS	VSS	AK41
AC6	VSS	VSS	AK48
AD13	VSS	VSS	AK53
AD16	VSS	VSS	AL14
AD18	VSS	VSS	AL17
AD21	VSS	VSS	AL19
AD23	VSS	VSS	AL2
AD26	VSS	VSS	AL22
AD28	VSS	VSS	AL24
AD31	VSS	VSS	AL27
AD33	VSS	VSS	AL30
AD36	VSS	VSS	AL32
AD38	VSS	VSS	AL35
AD41	VSS	VSS	AL37
AD48	VSS	VSS	AL40
AD53	VSS	VSS	AL45
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AMETHYST_BGA1737_HCBGA_AMETHYST_XT
OMIT_TABLE

U8700
AMETHYST_XT
HCBGA
SYM 13 OF 15
GND 2

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AT49	VSS	VSS	BA24
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AV14	VSS	VSS	BC16
AV17	VSS	VSS	BC19
AV19	VSS	VSS	BC2
AV22	VSS	VSS	BC23
AV24	VSS	VSS	BC28
AV27	VSS	VSS	BC33
AV30	VSS	VSS	BC40
AV32	VSS	VSS	BC46
AV35	VSS	VSS	BC50
AV37	VSS	VSS	BC6
AV40	VSS	VSS	BD15
AV43	VSS	VSS	BD18
AV46	VSS	VSS	BD29
AV8	VSS	VSS	BD38
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AMETHYST_XT
HCBGA
SYM 14 OF 15
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BE25	VSS	VSS	F39
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BE8	VSS	VSS	F47
BF14	VSS	VSS	F7
BF16	VSS	VSS	G2
BF19	VSS	VSS	G29
BF21	VSS	VSS	G48
BF26	VSS	VSS	G52
BF32	VSS	VSS	G6
BF35	VSS	VSS	H12
BF42	VSS	VSS	H16
BF53	VSS	VSS	H21
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BG35	VSS	VSS	H35
BG40	VSS	VSS	H38
BG6	VSS	VSS	H42
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BH11	VSS	VSS	H9
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BH14	VSS	VSS	J18
BH15	VSS	VSS	J2
BH24	VSS	VSS	J22
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BH31	VSS	VSS	J33
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BK39	VSS	VSS	K6
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BM7	VSS	VSS	M16
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C3	VSS	VSS	N52
C51	VSS	VSS	P13
D1	VSS	VSS	P16
D53	VSS	VSS	P18
F10	VSS	VSS	P21
F11	VSS	VSS	P23
F14	VSS	VSS	P26
F15	VSS	VSS	P28
F18	VSS	VSS	P31
F19	VSS	VSS	P33
F23	VSS	VSS	P36
F27	VSS	VSS	P38

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AMETHYST_XT
HCBGA
SYM 15 OF 15
GND 4

P41	VSS	
P46	VSS	
P48	VSS	
P6	VSS	
P9	VSS	
R10	VSS	
R2	VSS	
R44	VSS	
R48	VSS	
R50	VSS	
R6	VSS	
T11	VSS	
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T8	VSS	
U13	VSS	
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U2	VSS	
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DRAWING LAST_MODIFIED=Thu Feb 26 18:43:01 2015
SYNC_MASTER=J78_PETER SYNC_DATE=11/13/2013

PAGE TITLE
GRAPHICS: GPU GNDS & UNUSED

Apple Inc.

DRAWING NUMBER 051-00321
SIZE D
REVISION 4.0.0
BRANCH proto1b
PAGE 99 OF 120
SHEET 85 OF 96

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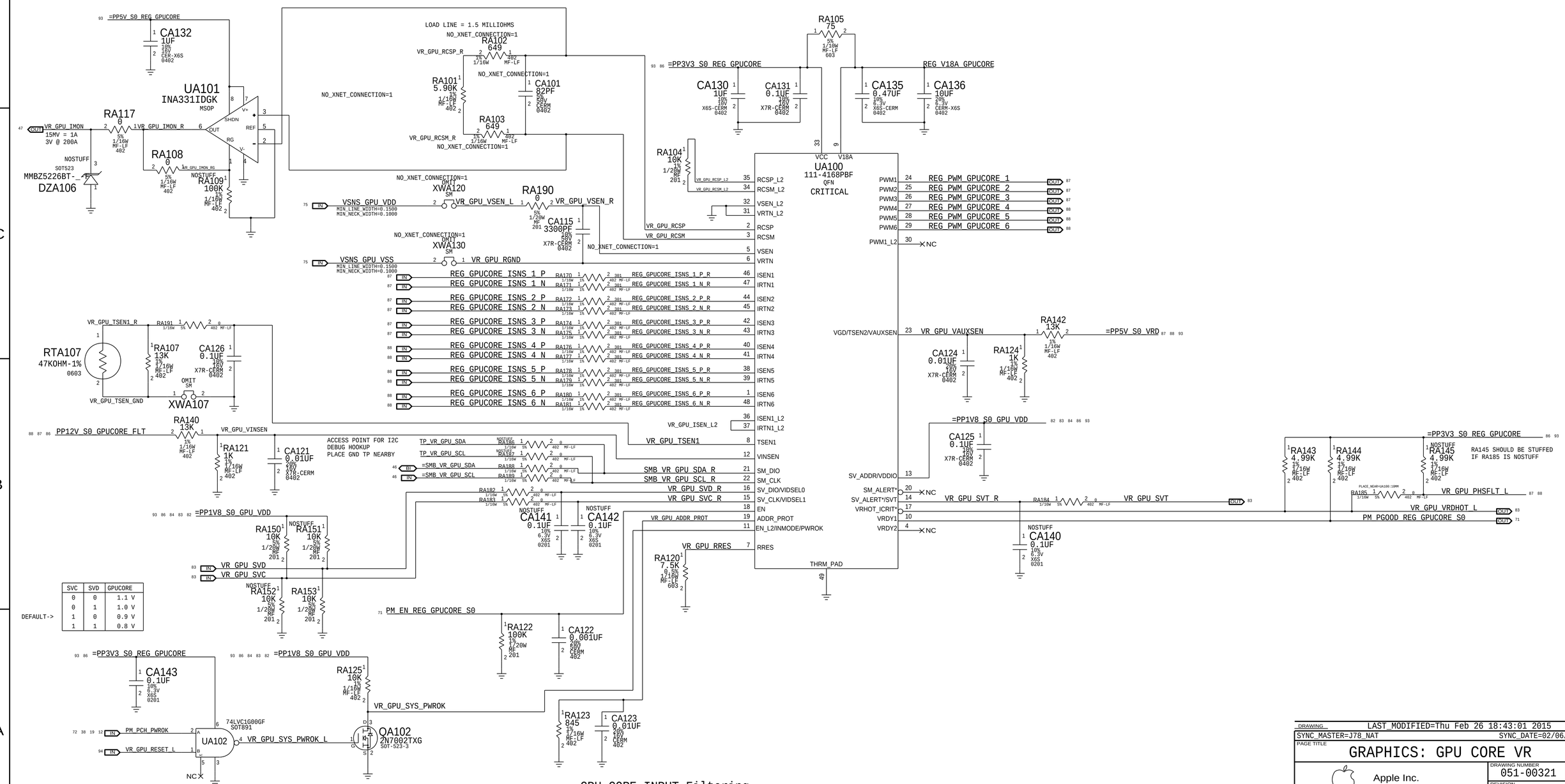
O/P= PPGPUCORE_S0_REG

GPUCORE
VOUT = VCORE
PEAK = 195A
AVG = 154A



SVC	SVD	GPUCORE
0	0	1.1 V
0	1	1.0 V
1	0	0.9 V
1	1	0.8 V

DEFAULT->

DRAWING	LAST_MODIFIED=Thu Feb 26 18:43:01 2015
SYNC_MASTER=J78_NAT	SYNC_DATE=02/06/2014
PAGE TITLE	GRAPHICS: GPU CORE VR
Apple Inc.	DRAWING NUMBER 051-00321 SIZE D
	REVISION 4.0.0
	BRANCH proto1b
	PAGE 101 OF 120
	SHEET 86 OF 96

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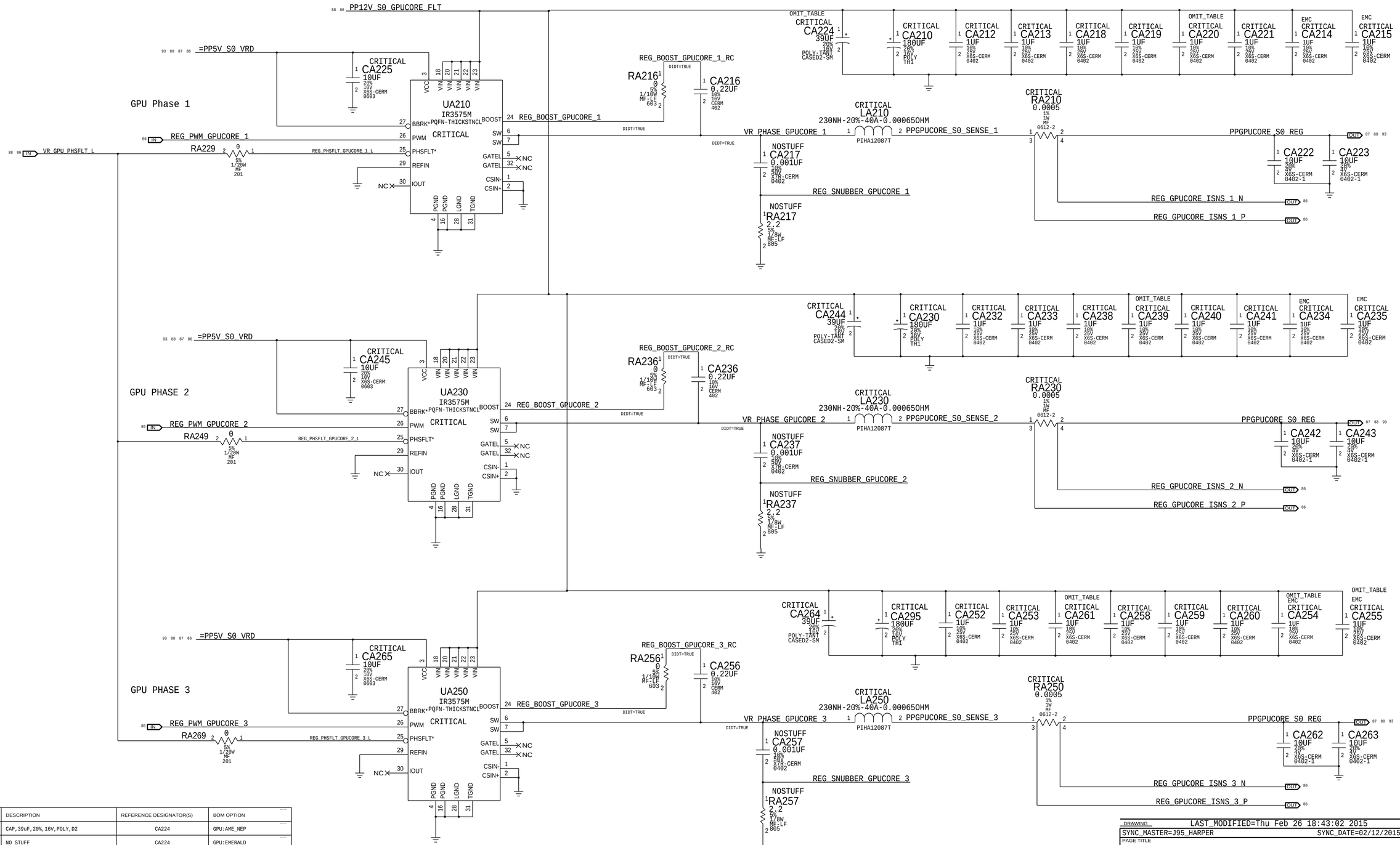

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0315	1	CAP,39uF,20%,16V,POLY,D2	CA224	GPU:AME_NEP
	1	NO STUFF	CA224	GPU:EMERALD
138S0775	5	CAP,1uF,10%,25V,X6S,0402	CA254,CA220,CA255,CA239,CA261	GPU:AME_NEP
	5	NO STUFF	CA254,CA220,CA255,CA239,CA261	GPU:EMERALD

DRAWING LAST_MODIFIED=Thu Feb 26 18:43:02 2015

SYNC_MASTER=J95_HARPER SYNC_DATE=02/12/2015

PAGE TITLE

GRAPHICS: GPU CORE VR (PHASES 1-3)

Apple Inc.

DRAWING NUMBER 051-00321 SIZE D

REVISION 4.0.0

BRANCH proto1b

PAGE 102 OF 120

SHEET 87 OF 96

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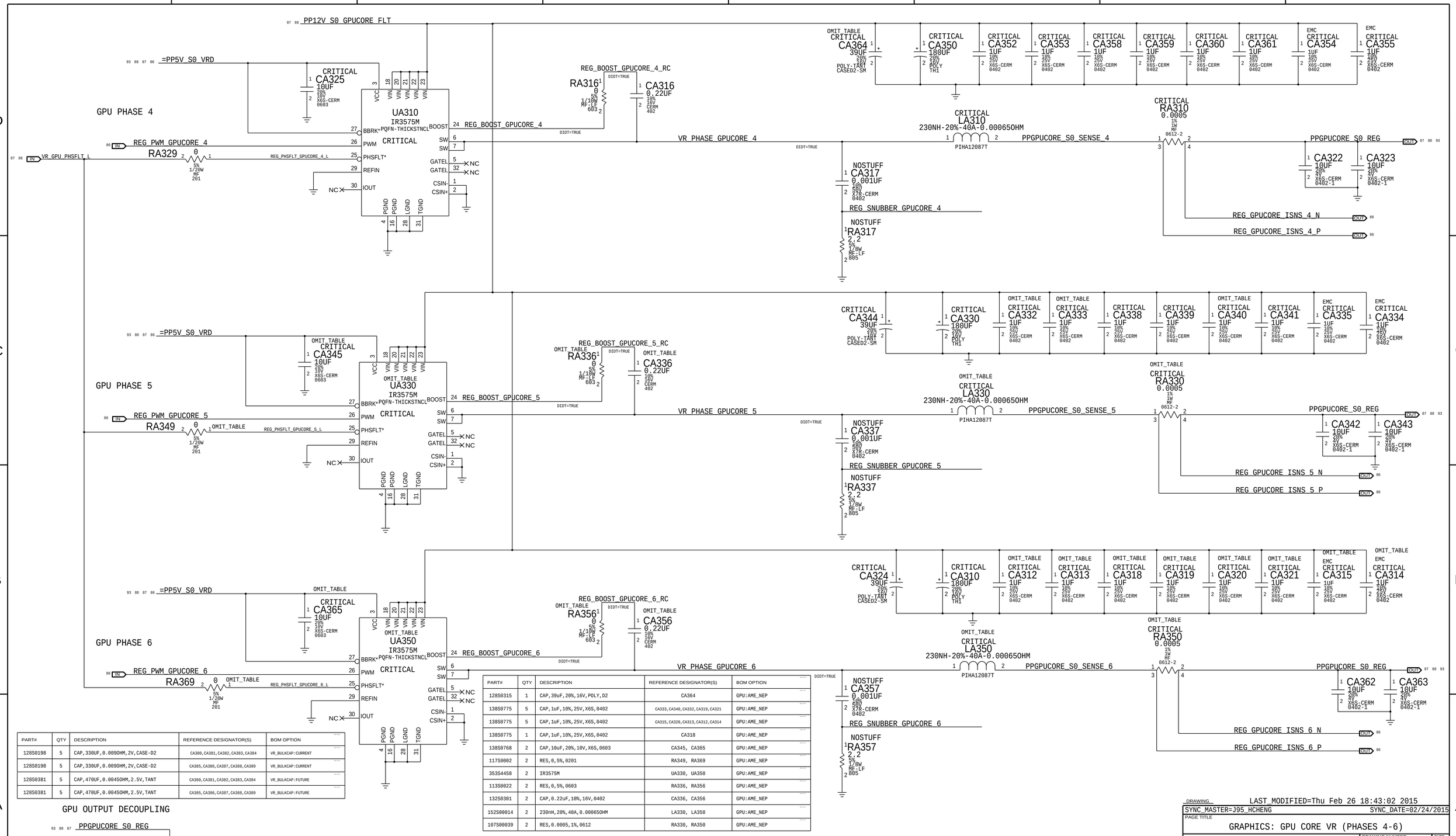

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0198	5	CAP,330UF,0.0090HM,2V,CASE-D2	CA380,CA381,CA382,CA383,CA384	VR_BULKCAP:CURRENT
128S0198	5	CAP,330UF,0.0090HM,2V,CASE-D2	CA385,CA386,CA387,CA388,CA389	VR_BULKCAP:CURRENT
128S0381	5	CAP,470UF,0.00450HM,2.5V,TANT	CA380,CA381,CA382,CA383,CA384	VR_BULKCAP:FUTURE
128S0381	5	CAP,470UF,0.00450HM,2.5V,TANT	CA385,CA386,CA387,CA388,CA389	VR_BULKCAP:FUTURE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0315	1	CAP,39uF,20%,16V,POLY,D2	CA364	GPU:AME_NEP
138S0775	5	CAP,1uF,10%,25V,X6S,0402	CA333,CA340,CA332,CA319,CA321	GPU:AME_NEP
138S0775	5	CAP,1uF,10%,25V,X6S,0402	CA315,CA320,CA313,CA312,CA314	GPU:AME_NEP
138S0775	1	CAP,1uF,10%,25V,X6S,0402	CA318	GPU:AME_NEP
138S0768	2	CAP,10uF,20%,10V,X6S,0603	CA345, CA365	GPU:AME_NEP
117S0002	2	RES,0,5%,0201	RA349, RA369	GPU:AME_NEP
353S4458	2	IR3575M	UA330, UA350	GPU:AME_NEP
113S0022	2	RES,0,5%,0603	RA336, RA356	GPU:AME_NEP
132S0301	2	CAP,0.22uF,10%,16V,0402	CA336, CA356	GPU:AME_NEP
152S00014	2	230nH,20%,40A,0.000650HM	LA330, LA350	GPU:AME_NEP
107S00039	2	RES,0.0005,1%,0612	RA330, RA350	GPU:AME_NEP

GPU OUTPUT DECOUPLING

PPGPUCORE_S0_REG

CA380 CA381 CA382 CA383 CA384 CA385 CA386 CA387 CA388 CA389
470UF-0.00450HM
POLY-TANT
SM

DRAWING LAST_MODIFIED=Thu Feb 26 18:43:02 2015
SYNC_MASTER=J95_HCHENG SYNC_DATE=02/24/2015
PAGE TITLE
GRAPHICS: GPU CORE VR (PHASES 4-6)

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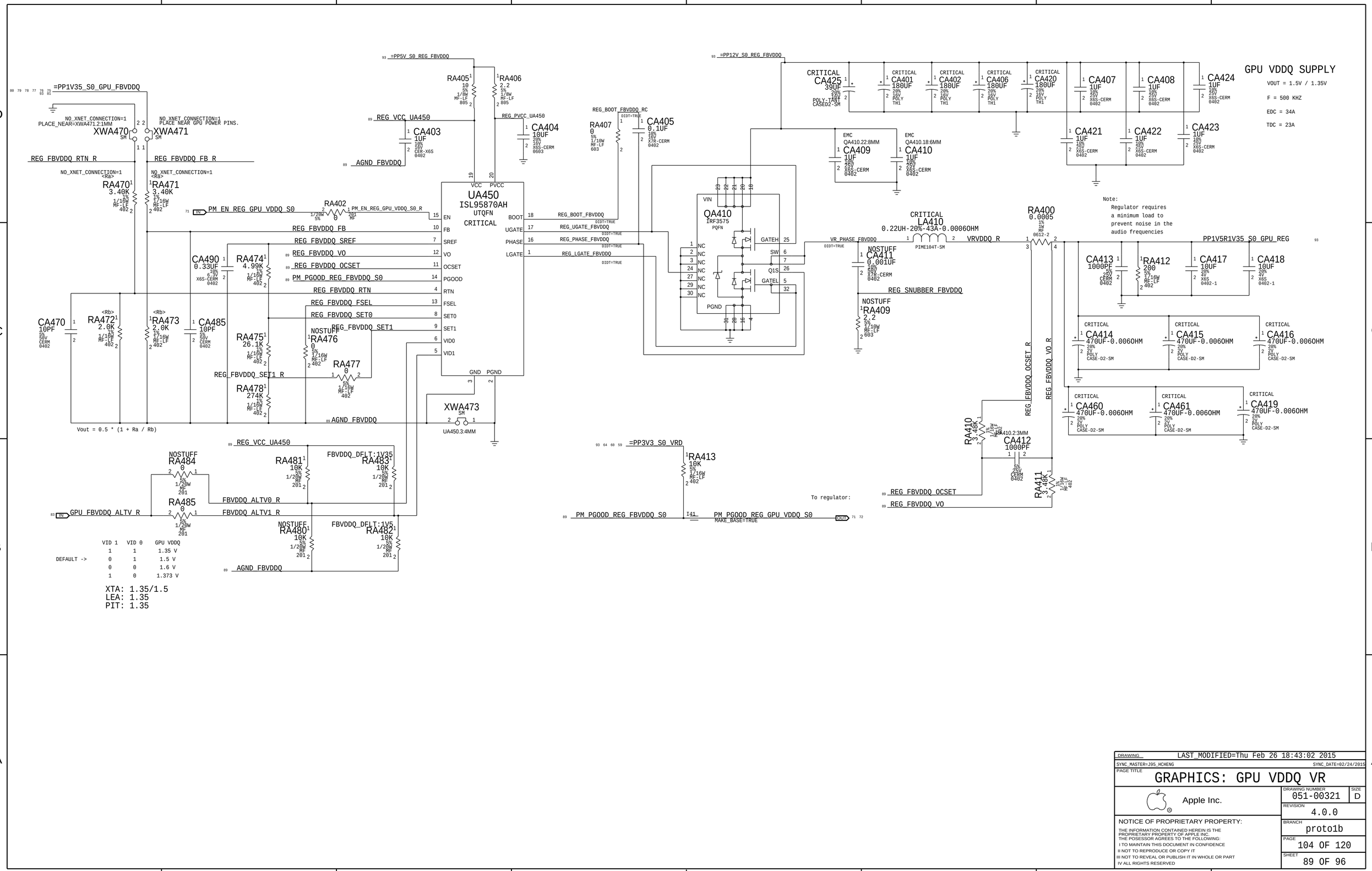
GPU VDDQ SUPPLY
VOUT = 1.5V / 1.35V
F = 500 KHZ
EDC = 34A
TDC = 23A
UA450
ISL95870AH
UTQFN
CRITICAL
QA410
IRF3575
PQFN
LA410
0.22UH-20%-43A-0.0006OHM
PIME104T-SM
Note:
Regulator requires
a minimum load to
prevent noise in the
audio frequencies
Vout = 0.5 * (1 + Ra / Rb)
VID 1 VID 0 GPU VDDQ
1 1 1.35 V
0 1 1.5 V
0 0 1.6 V
1 0 1.373 V
DEFAULT ->
XTA: 1.35/1.5
LEA: 1.35
PIT: 1.35
To regulator:
DRAWING
LAST_MODIFIED=Thu Feb 26 18:43:02 2015
SYNC_MASTER=J95_HCHENG
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PAGE TITLE
GRAPHICS: GPU VDDQ VR
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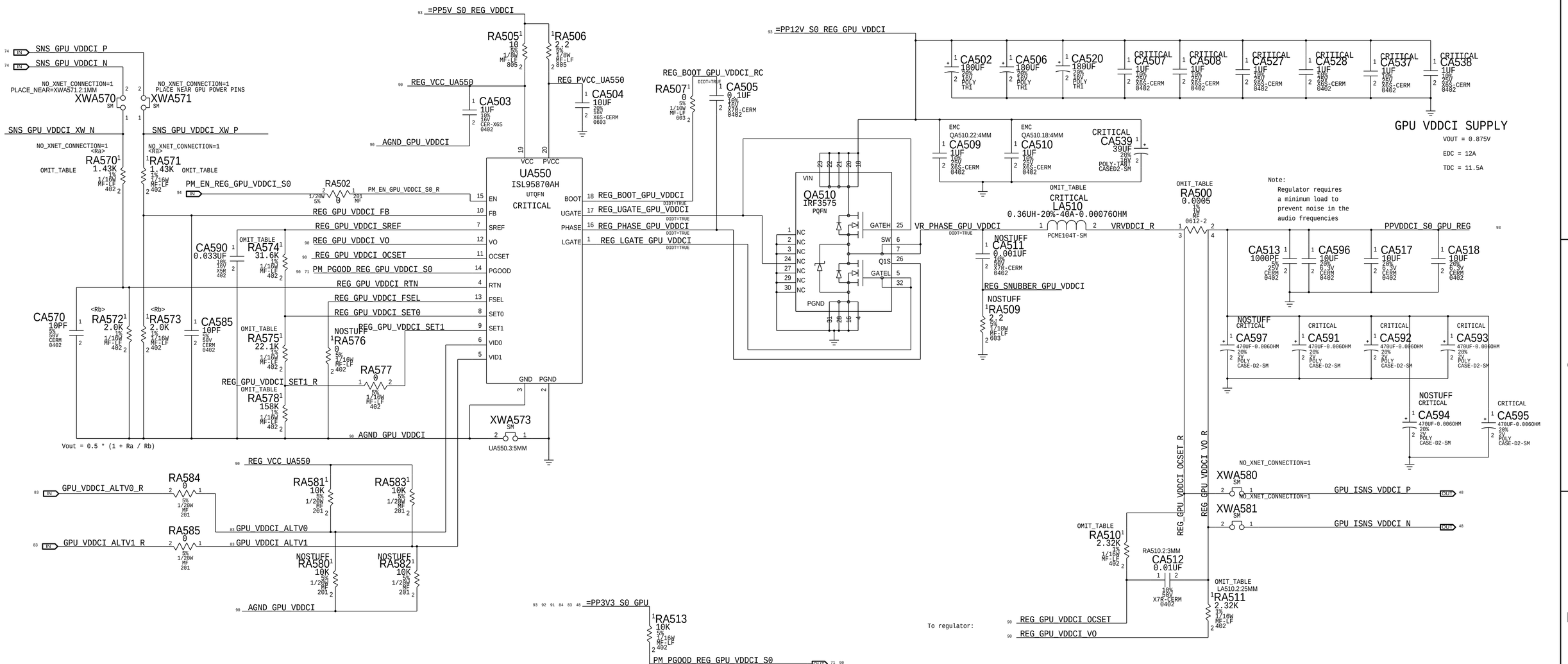

NEPTUNE

	VID 1	VID 0	GPU VDDCI
DEFAULT ->	1	1	0.850 V
	1	0	1.000 V

AMETHYSTP_XTA

	VID 1	VID 0	GPU VDDCI
DEFAULT ->	1	1	0.825 V
	1	0	0.950 V
	0	1	1.000 V

AMETHYSTP_PROA

	VID 1	VID 0	GPU VDDCI
DEFAULT ->	1	1	0.825 V
	1	0	0.925 V
	0	1	1.050 V

EMERALD

	VID 1	VID 0	GPU VDDCI
DEFAULT ->	1	1	0.800 V
	1	0	0.925 V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0363	1	RES,31.6K,0402	RA574	GPU:EMERALD_PROA
116S0068	2	RES,1.2K,0402	RA570,RA571	GPU:EMERALD_PROA
114S0378	1	RES,45.3K,0402	RA575	GPU:EMERALD_PROA
114S0363	1	RES,31.6K,0402	RA574	GPU:NEPTUNE_PROA
114S0231	2	RES,1.4K,0402	RA570,RA571	GPU:NEPTUNE_PROA
114S0347	1	RES,22.1K,0402	RA575	GPU:NEPTUNE_PROA
114S0386	1	RES,53.6K,0402	RA574	GPU:AM_XTA
114S0228	2	RES,1.3K,0402	RA570,RA571	GPU:AM_XTA
114S0339	1	RES,18.2K,0402	RA575	GPU:AM_XTA
114S0386	1	RES,53.6K,0402	RA574	GPU:AM_PROA
114S0228	2	RES,1.3K,0402	RA570,RA571	GPU:AM_PROA
114S0364	1	RES,32.4K,0402	RA575	GPU:AM_PROA
114S0430	1	RES,158K,0402	RA578	GPU:EMERALD_PROA
114S0430	1	RES,158K,0402	RA578	GPU:NEPTUNE_PROA
114S0463	1	RES,340K,0402	RA578	GPU:AM_XTA
114S0460	1	RES,316K,0402	RA578	GPU:AM_PROA

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S1799	1	IND,0.36UH,40A,0.8MOHM	LA510	GPU:AME_NEP
152S1783	1	IND,0.68UH,28A,1.75MOHM	LA510	GPU:EMERALD
107S00039	1	RES,0.0005OHM,1%,0612-4T	RA500	GPU:AME_NEP
107S0255	1	RES,0.001OHM,1%,0612-4T	RA500	GPU:EMERALD
114S0252	2	RES,2.32K,1%,0402	RA510,RA511	GPU:AME_NEP
114S0251	2	RES,2.26K,1%,0402	RA510,RA511	GPU:EMERALD

SYNC_MASTER=J95_HCHENG SYNC_DATE=02/24/2015

PAGE TITLE
GRAPHICS: GPU VDDCI VR

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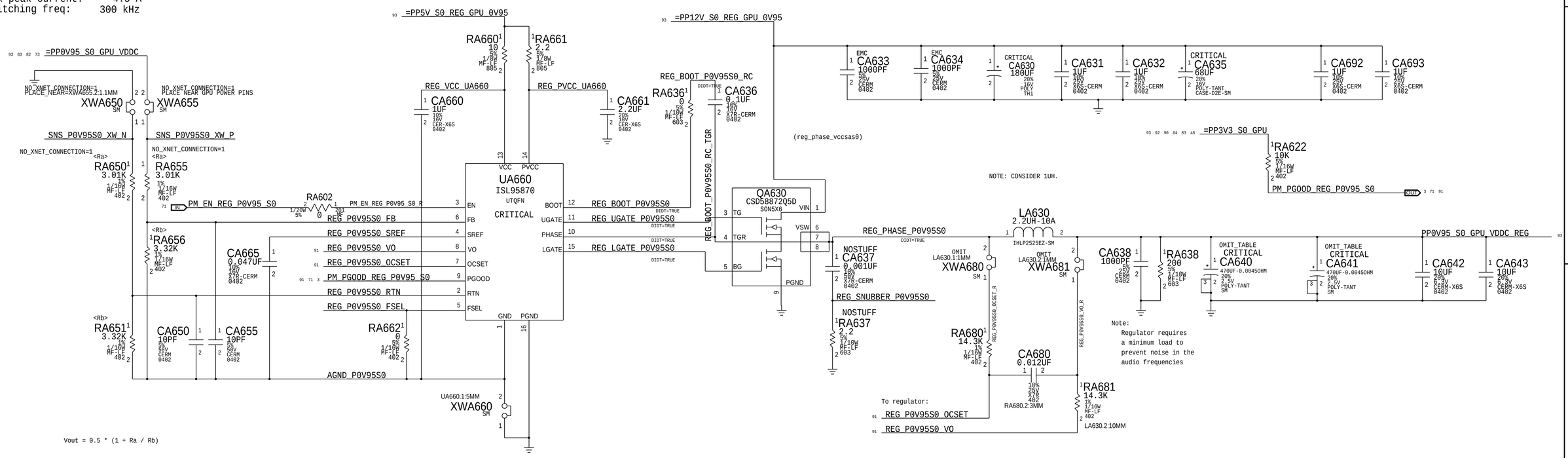
GPU VDDC (0.95V) S0 REGULATOR

Max avg current: 4.3 A
Max peak current: 4.5 A
Switching freq: 300 kHz



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0358	2	CAP,470uF,0.0060HM,2V,D2	CA640,CA641	VR_BULKCAP:CURRENT
128S0381	2	CAP,470uF,0.00450HM,2.5V,SM	CA640,CA641	VR_BULKCAP:FUTURE

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PAGE TITLE
GRAPHICS: GPU 0V95 VR

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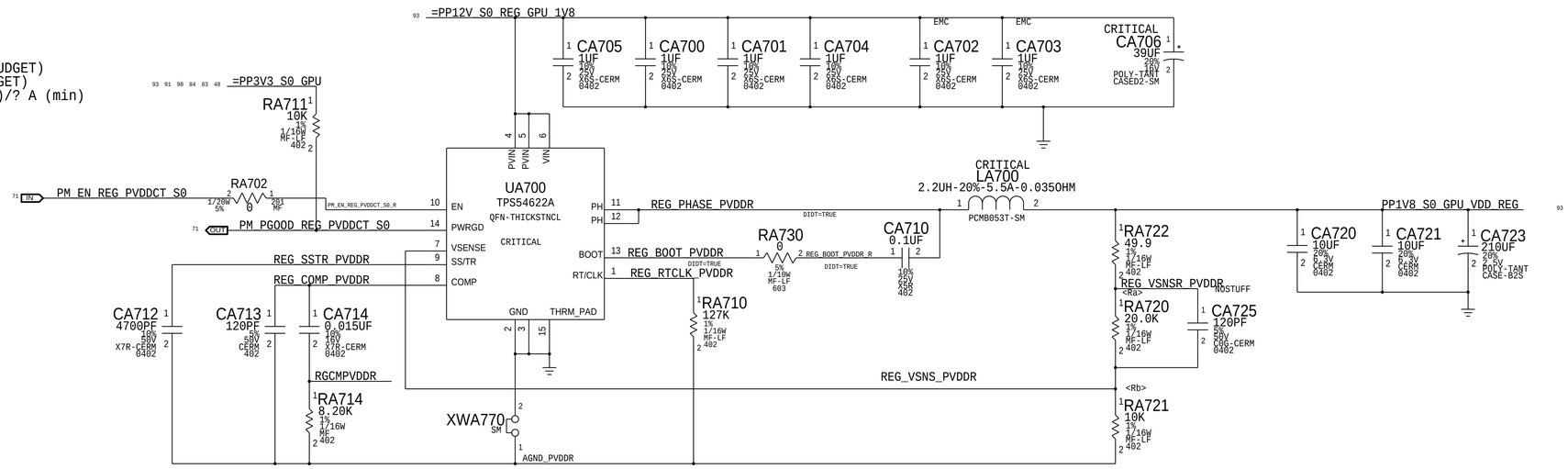
1.8V S0 Regulator

Max avg current: 2.4 A (BUDGET)
Max peak current: 3 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz



VOUT = 0.6 * (1 + RA / RB)

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SYNC_MASTER=J95_HARPER	SYNC_DATE=02/11/2015
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G3 Rails

Always on: Keeps the PCH RTC alive

PP3V3_G3 (MAKE_BASE=TRUE)	PP3V3_G3_RTC	18
	=PP3V3_G3_PCH_RTC	12 15

G3H Rails

On with AC/DC plugged in

PP12V_ACDC (MAKE_BASE=TRUE)	PP12V_G3H_ACDC	59
	=PP12V_G3H_SNS_R	47
PP12V_G3H (MAKE_BASE=TRUE)	PP12V_G3H_SNS	47
	=PP12V_G3H_P3V42	59
	=PP12V_G3H_FET_P12V_S0	70
	=PP12V_G3H_FET_P12V_S5	70
	=PP12V_G3H_FET_P12V_S5_SSD	65 70
PP3V42_G3H (MAKE_BASE=TRUE)	PP3V42_G3H_REG	59
	=PP3V3_G3H_BT	31
	=PP3V3_G3H_RTC_D	18
	=PP3V3_G3H_SMC	43 44 50
	=PP3V3_G3H_SMC_USBMUX	41
	=PPVIN_G3H_SMCVREF	44
	=PP3V3_G3H_T112	45
	=PP3V3_G3H_SSD	59 65 70

Ground/Common

GND (MAKE_BASE=TRUE)	⏚

S5 Rails

On when in S5

PP12V_S5 (MAKE_BASE=TRUE)	PP12V_S5_FET	70
	=PP12V_S5_REG_VDDQ_S3	63
	=PP12V_S5_PWRCTL	70 71
	=PPHV_SW_TBTAPWRSW	28
	=PPHV_SW_TBTBPWRSW	29
	=PP12V_S5_SNS	47
	=PP12V_S5_REG_P1V0_S5	66
PP12V_S5_SSD (MAKE_BASE=TRUE)	PP12V_S5_SSD_FET	70
	=PP12V_S5_FET_P3V3_S5_P5V_S4	65
	=PP12V_S5_FET_PWRCTL	32 70
	=PP12V_S5_FET_P12V_S5_NON_SSD	65
PP5V_S5 (MAKE_BASE=TRUE)	PP5V_S5_LDO	65
	=PP5V_S5_REG_P1V0	66
	=PP5V_S5_XDP	17
PP3V3_S5 (MAKE_BASE=TRUE)	PP3V3_S5_FET_NON_SSD	65
	=PP3V3_S5_FET_P3V3_S0	70
	=PP3V3_S5_FET_P3V3_S4	70
	=PP3V3_S5_SMC	32 44
	=PP3V3_S5_LED	3
	=PP3V3_S5_PCH_VCC	12 13 14 15 18 19
	=PP3V3_S5_PWRCTL	32 65 71 72
	=PP3V3_S5_ROM	17 45
	=PP3V3_S5_VRD	65 66
	=PP3V3_S5_SENSE	47
	=PP3V3_S5_RSTBUF	19
PP3V3_S5_SSD (MAKE_BASE=TRUE)	PP3V3_S5_REG_SSD	65
	=PPVSSD_S5_FET_S4_SSD	32
	=PP3V3_S5_SSD_PWRCTL	32 65
	=PP3V3_S5_NON_SSD	65
PP1V0_S5 (MAKE_BASE=TRUE)	PP1V0_S5_REG	66
	=PP1V0_S5_PCH_VCC	11 15
	=PP1V0_S5_XDP	17
	=PP1V0_S5_FET_PP1V0_S3	70

S4 Rails

Enabled when system has AC and is in run or sleep

PP5V_S4 (MAKE_BASE=TRUE)	PP5V_S4_REG	65
	=PP5V_S4_REG_VDDQ_S3	63
	=PP5V_S4_FET_P5V_S0	70
	=PP5V_S4_USB	41 42
PP3V3_S4 (MAKE_BASE=TRUE)	PP3V3_S4_FET	70
	=PP3V3_S4_FET_ENET	35
	=PP3V3_S4_PWRCTL	41 42 63 70
	=PP3V3_S4_LED	3
	=PP3V3_S4_MEMRESET	6
	=PP3V3_S4_PCH_VCC	13 14
	=PP3V3_S4_SDCARD	36
	=PP3V3_S4_SMC	44
	=PP3V3_S4_TBT	19 26 27 28 29 30 71
	=PP3V3_S4_AUDIO_DIG	55
	=PP3V3_S4_TBTAPWRSW	28
	=PP3V3_S4_TBTBPWRSW	29
	=PP3V3_S4_AP	31 44
PP3V3_S4_SSD_FET (MAKE_BASE=TRUE)	PP3V3_S4_FET_SSD	32
	=PPVSSD_S4_REG_SNS_R	48
PP3V3_S4_SSD (MAKE_BASE=TRUE)	PPVSSD_S4_REG_SNS	48
	=PPVSSD_S4_CONN	32

S3 Rails

Enabled when system is in run or sleep

PP3V3_ENET (MAKE_BASE=TRUE)	PP3V3_ENET_FET	35
	=PP3V3_ENET_PHY	34 35
PPVDDQ_S3 (MAKE_BASE=TRUE)	PPVDDQ_S3_REG	63
	=PPVDDQ_S3_SNS_DDR_R	48
THIS IS 1.35V RAIL	=PP1V35_S3_SNS_R	48
PPVDDQ_S3_DDR (MAKE_BASE=TRUE)	PPVDDQ_S3_SNS_DDR	48
	=PPDDR_S3_MEMVREF	20
THIS IS 1.35V RAIL	=PPVDDQ_S3_MEM_A	21 22
	=PPVDDQ_S3_MEM_B	23 24
	=PPVDDQ_S3_MEMRESET	12
	=PPVDDQ_S3_LDO_DDRVTT	63
PP1V35_S3_CPU (MAKE_BASE=TRUE)	PP1V35_S3_SNS	48
	=PPVDDQ_S3_CPU	8 10
PP1V0_S3_CPU_VCCST (MAKE_BASE=TRUE)	PP1V0_S3_FET	70
	=PP1V0_S3_VCCST	12 60
	=PP1V0_S3_SMC	44
	=PP1V0_S3_XDP	17
	=PP1V0_S3_CPU	6 8 10

S0 Rails

Enabled when system is in run

PP12V_S0 (MAKE_BASE=TRUE)	PP12V_S0_FET	70
	=PP12V_S0_AUDIO_SPKRAMP	53 54
	=PP12V_S0_FAN	50
	=PP12V_S0_SNS_GPUCORE_R	47
	=PP12V_S0_LCD	39
	=PP12V_S0_CPUCORE	60
	=PP12V_S0_SNS_FBVDDQ_R	47
	=PP12V_S0_HDD	33
	=PP12V_S0_BKLT	68
PP12V_S0_GPU_AUX (MAKE_BASE=TRUE)	PP12V_S0_SNS_GPU_AUX	47
	=PP12V_S0_REG_GPU_0V95	91
	=PP12V_S0_REG_GPU_1V8	92
PP12V_S0_GPUCORE (MAKE_BASE=TRUE)	PP12V_S0_SNS_GPUCORE	47
	=PP12V_S0_REG_GPUCORE	86
	=PP12V_S0_REG_GPU_VDDCI	90
93 60 PP12V_S0_CPUCORE_FLT (MAKE_BASE=TRUE)	PP12V_S0_CPUCORE_FLT	60 93
	=PP12V_S0_SNS_CPUCORE_R	47
PP12V_S0_CPUCORE (MAKE_BASE=TRUE)	PP12V_S0_SNS_CPUCORE	47
	=PP12V_S0_REG_CPUCORE	60 61 62 64 67
PPHDD12_S0 (MAKE_BASE=TRUE)	PP12V_S0_HDD_FET	33
	=PP12V_S0_HDD_SNS_R	48
PP12V_S0_HDD (MAKE_BASE=TRUE)	PP12V_S0_HDD_SNS	48
	=PP12V_S0_HDD_PWR	33
PP12V_S0_FBVDDQ (MAKE_BASE=TRUE)	PP12V_S0_SNS_FBVDDQ	47
	=PP12V_S0_REG_FBVDDQ	89
PP5V_S0 (MAKE_BASE=TRUE)	PP5V_S0_FET	70
	=PP5V_S0_AUDIO	51 58
	=PP5V_S0_BKLT	68
	=PP5V_S0_ISENSE	47
	=PP5V_S0_REG_CPUVCC_S0	60 61 62 64 67
	=PP5V_S0_REG_FBVDDQ	89
	=PP5V_S0_HDD	33
	=PP5V_S0_VRD	86 87 88
	=PP5V_S0_REG_VDDCI	90
	=PP5V_S0_REG_GPU_0V95	91
	=PP5V_S0_CAMERA	37
	=PP5V_S0_REG_GPUCORE	86
PPHDD_S0 (MAKE_BASE=TRUE)	PP5V_S0_HDD_FET	33
	=PPHDD_S0_SNS_R	48
PP5V_S0_HDD (MAKE_BASE=TRUE)	PPHDD_S0_SNS	48
	=PP5V_S0_HDD_PWR	33
PP3V3_S0 (MAKE_BASE=TRUE)	PP3V3_S0_FET	70
	=PP3V3_S0_AUDIO	37 51 53 54 57
	=PP3V3_S0_AUDIO_DIG	55
	=PP3V3_S0_BKLT	68
	=PP3V3_S0_DP	30 39
	=PP3V3_S0_ENET	34
	=PP3V3_S0_FAN	50
	=PP3V3_S0_GPU	48 83 84 90 91 92
	=PP3V3_S0_INTDPMUX	39 40
	=PP3V3_S0_LED	3
	=PP3V3_S0_LED_SATA	32
	=PP3V3_S0_MEM_A_SPD	21 22
	=PP3V3_S0_MEM_B_SPD	23 24
	=PP3V3_S0_PCH_VCC	11 12 14 15 18 19
	=PP3V3_S0_PWRCTL	70 71
	=PP3V3_S0_RSTBUF	19
	=PP3V3_S0_SDCARD	36
	=PP3V3_S0_SENSE	33 47 48 49
	=PP3V3_S0_SMBUS	46
	=PP3V3_S0_SMBUS_SMC_0	46
	=PP3V3_S0_SMBUS_SMC_1	46
	=PP3V3_S0_SMBUS_SMC_3	46
	=PP3V3_S0_SMC	44
	=PP3V3_S0_VRD	59 60 64 89
	=PP3V3_S0_PCH_GPIO	27
	=PP3V3_S0_CAMERA	37 38
	=PP3V3_S0_ALS	37
	=PP3V3_S0_SMBUS_SMC_2	46
	=PP3V3_S0_REG_GPUCORE	86
PPDDRVTT_S0 (MAKE_BASE=TRUE)	PPDDRVTT_S0_LDO	63
	=PPDDRVTT_S0_MEM_A	21 22
	=PPDDRVTT_S0_MEM_B	23 24

GPU Rails (S0)

Enabled when system is in run

PPGPUCORE_S0 (MAKE_BASE=TRUE)	PPGPUCORE_S0_REG	87 88
	=PPGPUCORE_S0	74 75
	=PPGPUCORE_S0_SNS	47
FBVDDQ IS 1.5V		
PPFBVDDQ_S0_GPU (MAKE_BASE=TRUE)	PP1V5R1V35_S0_GPU_REG	89
	=PP1V35_S0_GPU_FBVDDQ	75 76 77 78 79 80 81 89
PPVDDCI_S0_GPU (MAKE_BASE=TRUE)	PPVDDCI_S0_GPU_REG	90
	=PPVDDCI_S0_GPU	74
PP0V95_S0_GPU_VDDC (MAKE_BASE=TRUE)	PP0V95_S0_GPU_VDDC_REG	91
	=PP0V95_S0_GPU_VDDC	73 82 83 91
	=PP0V95_S0_GPU_PCIEVDDC	73
PP1V8_S0_MISC (MAKE_BASE=TRUE)	PP1V8_S0_GPU_VDD_REG	92
	=PP1V8_S0_GPU_VDD	82 83 84 86
	=PP1V8_S0_CAMERA	37 38
	=PP1V8_S0_GPU_PEX_IO	73
	=PP1V8_S0_AUD_DIG	51
	=PP1V8_S0_DP	40

Thunderbolt Rails (S0)

Enabled when Thunderbolt cable is plugged in

27 26 PP3V3_TBTLC (MAKE_BASE=TRUE)	=PP3V3_TBTLC	19

CPU/PCH Rails (S0)

Enabled when system is in run

PPVCC_S0_CPU (MAKE_BASE=TRUE)	PPVCC_S0_CPU_REG	61
	=PPVCC_S0_CPU	8 10
	=PPVCC_S0_SNS_CPU	47
PPVCCGT_S0_CPU (MAKE_BASE=TRUE)	PPVCCGT_S0_CPU_REG	62
	=PPVCCGT_S0_CPU	8 10
	=PPVCCGT_S0_SNS_CPU	47
PPVCCSA_S0_CPU (MAKE_BASE=TRUE)	PPVCCSA_S0_CPU_REG	67
	=PPVCCSA_S0_CPU	8 10
PPVCCIO_S0 (MAKE_BASE=TRUE)	PPVCCIO_S0_CPU_REG	64
	=PPVCCIO_S0_SNS_CPU_R	47
PPVCCIO_S0_CPU (MAKE_BASE=TRUE)	PPVCCIO_S0_SNS_CPU	47
	=PPVCCIO_S0_CPU	5 8 10 17

SYNC_MASTER=J78_MLB SYNC_DATE=11/20/2013

PAGE TITLE

Power Connectors/Aliases

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PEG aliases

```
73 PEG_D2R_N<0..15>      ==  =PEG_D2R_N<15..0>     5
                MAKE_BASE=TRUE ==
73 PEG_D2R_P<0..15>      ==  =PEG_D2R_P<15..0>     5
                MAKE_BASE=TRUE ==
73 PEG_R2D_C_N<0..15>    ==  =PEG_R2D_C_N<15..0>   5
                MAKE_BASE=TRUE ==
73 PEG_R2D_C_P<0..15>    ==  =PEG_R2D_C_P<15..0>   5
                MAKE_BASE=TRUE ==
```

GPU ALIASES

```
83 73 GPU_RESET_L        ==  TP_GPU_RESET_L        19
                MAKE_BASE=TRUE ==
   86 VR_GPU_RESET_L     ==  TP_VR_GPU_RESET_L     19
                MAKE_BASE=TRUE ==
```

GPU VDDCI PGOOD

```
71 TP_PM_EN_REG_GPU_VDDCI_S0  ==  PM_EN_REG_GPU_VDDCI_S0   90
                                  MAKE_BASE=TRUE
```

SYNC_MASTER=J78_MLB SYNC_DATE=12/05/2013

PAGE TITLE

Signal Aliases

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CPU Reserved

17 6 CPU_CFG<15..12> — TP_CPU_CFG<15..12>
MAKE_BASE=TRUE

39 DP_INT_PIN_57 — NC_DP_INT_PIN_57
MAKE_BASE=TRUE

39 DP_INT_PIN_55 — NC_DP_INT_PIN_55
MAKE_BASE=TRUE

12 TP_CLINK_DATA — CLINK_DATA
MAKE_BASE=TRUE NO_TEST=1

12 TP_CLINK_CLK — CLINK_CLK
MAKE_BASE=TRUE NO_TEST=1

12 TP_CLINK_RESET_L — CLINK_RESAT_L
MAKE_BASE=TRUE NO_TEST=1

83 TP_GPU_CB_REFCKN_OUT1 — GPU_CB_REFCKN_OUT1
MAKE_BASE=TRUE

83 TP_GPU_CB_REFCKP_OUT1 — GPU_CB_REFCKP_OUT1
MAKE_BASE=TRUE

83 TP_GPU_PLL_ANALOG_IN — GPU_PLL_ANALOG_IN
MAKE_BASE=TRUE

12 TP_PCH_SLP_LAN_L — PCH_SLP_LAN_L
MAKE_BASE=TRUE NO_TEST=1

11 TP_PCH_2 — PCH_2
MAKE_BASE=TRUE NO_TEST=1

12 TP_PM_SLP_A_L — PM_SLP_A_L
MAKE_BASE=TRUE NO_TEST=1

26 TP_TBT_MONDC1 — TBT_MONDC1
MAKE_BASE=TRUE

26 TP_TBT_PCIE_RESET0_L — TBT_PCIE_RESET0_L
MAKE_BASE=TRUE NO_TEST=1

PCH Clocks

TP_ITPXDP_CLK100MP — ITPXDP_CLK100M_P 11 17
MAKE_BASE=TRUE NO_TEST=1

TP_ITPXDP_CLK100MN — ITPXDP_CLK100M_N 11 17
MAKE_BASE=TRUE NO_TEST=1

PCH Miscellaneous

11 TP_HDA_SDIN1 — NC_HDA_SDIN1
MAKE_BASE=TRUE NO_TEST=1

11 PEG_CLKREQ_L — NC_PEG_CLKREQ_L
MAKE_BASE=TRUE

14 GPU_NEPTUNE_EMERALD_ID — NC_GPU_IS_AMETHYST
MAKE_BASE=TRUE NO_TEST=1

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Unused Signal Aliases

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J17 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA_TBT,BGA_VRAM	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	0.070 MM	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.185 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	ISL5,ISL8	Y	0.205 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.220 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.150 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	ISL5,ISL8	Y	0.165 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.130 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	ISL5,ISL8	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.155 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.115 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	ISL5,ISL8	Y	0.126 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.090 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	ISL5,ISL8	Y	0.100 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	ISL5,ISL8	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.171 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.085 MM	=STANDARD	0.150 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.136 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.141 MM	0.085 MM	=STANDARD	0.185 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.121 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.109 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.086 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.085 MM	=STANDARD	0.230 MM	0.1 MM

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_ISO	*	=STANDARD	8000
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

GENERIC

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GENERIC_ISO	*	=1:1_SPACING	?

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1X_DIELECTRIC	ISL3,ISL10	0.101 MM	?
1X_DIELECTRIC	*	0.076 MM	?

Board Stack-up

FINISHED BOARD THICKNESS: 1.94 MM

_____	Top	Signal	0.5 oz (Cu plated)
_____		Prepreg	0.071 MM
_____	2	Plane	1 oz
_____		Core	0.101 MM
_____	3	Signal	0.5 oz
_____		Prepreg	0.115 MM
_____	4	Plane	1 oz
_____		Core	0.076 MM
_____	5	Signal	0.5 oz
_____		Prepreg	0.380 MM
_____	6	Plane	1 oz
_____		Core	0.076 MM
_____	7	Plane	1 oz
_____		Prepreg	0.380 MM
_____	8	Signal	0.5 oz
_____		Core	0.076 MM
_____	9	Plane	1 oz
_____		Prepreg	0.115 MM
_____	10	Signal	0.5 oz
_____		Core	0.101 MM
_____	11	Plane	1 oz
_____		Prepreg	0.071 MM
_____	Btm	Signal	0.5 oz (Cu plated)

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J95 RULE DEFINITIONS

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